IH2657 Design of Nano Semi-conductor Devices 7.5 credits

Design av nanohalvledarkomponenter

This is a translation of the Swedish, legally binding, course syllabus.

If the course is discontinued, students may request to be examined during the following two academic years

Establishment

The official course syllabus is valid from the spring semester 2025 in accordance with the decision from the director of first and second cycle education: J-2024-1616.Decision date: 2024-10-15

Grading scale

A, B, C, D, E, FX, F

Education cycle

Second cycle

Main field of study

Electrical Engineering

Specific prerequisites

Knowledge in silicon-based semiconductor components, 7.5 higher education credits, equivalent to completed course IH1611.

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

After passing the course, the student shall be able to

- describe properties and limitations of a MOSFET transistor in an advanced CMOS technology node
- give an account of a methodological circuit design in nanometer CMOS technology that takes into account power consumption robustness, design rules, variations in device performance etc
- justify the need of new component and circuit topologies including 3D-fabrication
- give examples of components and materials that are appropriate to replace or would be complementary to silicon-based CMOS or charge based memories for example for low supply voltages or low power applications
- use physical and compact modelling to design components with desirable properties equivalent to a future technology node
- analyse and critically discuss research publications with regard to the relevance for technical development in the device field
- discuss advanced semiconductor fabrication from a sustainability perspective with a focus on energy consumption and other finite resources and raw materials.

Course contents

This course treats the most important component in all integrated circuits - the MOS-FET-transistor that is produced in silicon with nanometer dimensions. The focus is on low power CMOS-technology.

Course main content

- Basic physics for the MOS-system and formulation of approximate current-voltage relations for the MOS-transistor. Compact physics based models for circuit simulation. Modelling of process corners.
- Scaling theory and technology nodes for CMOS technology.
- Modern CMOS device topologies, SOI and FinFET, 3D-structures including nanowire/sheet.
- Power consumption, crosstalk and scaling of interconnects.
- Memory technologies, charge based, resistive or based on other physical principles.
- New technologies and applications as for instance spintronics, 2D-materials, and 3D-fabrication.
- Circuit design for nanometer CMOS, ASIC, FPGA, design rules, robustness, testing, reliability, error analysis, variability on component, chip and wafer level.

Examination

- LAB1 - Computer labs and home assignments, 3.0 credits, grading scale: P, F
- TENA - Written exam, 4.5 credits, grading scale: A, B, C, D, E, FX, F

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

TEN1 is replaced by TENA.

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.