

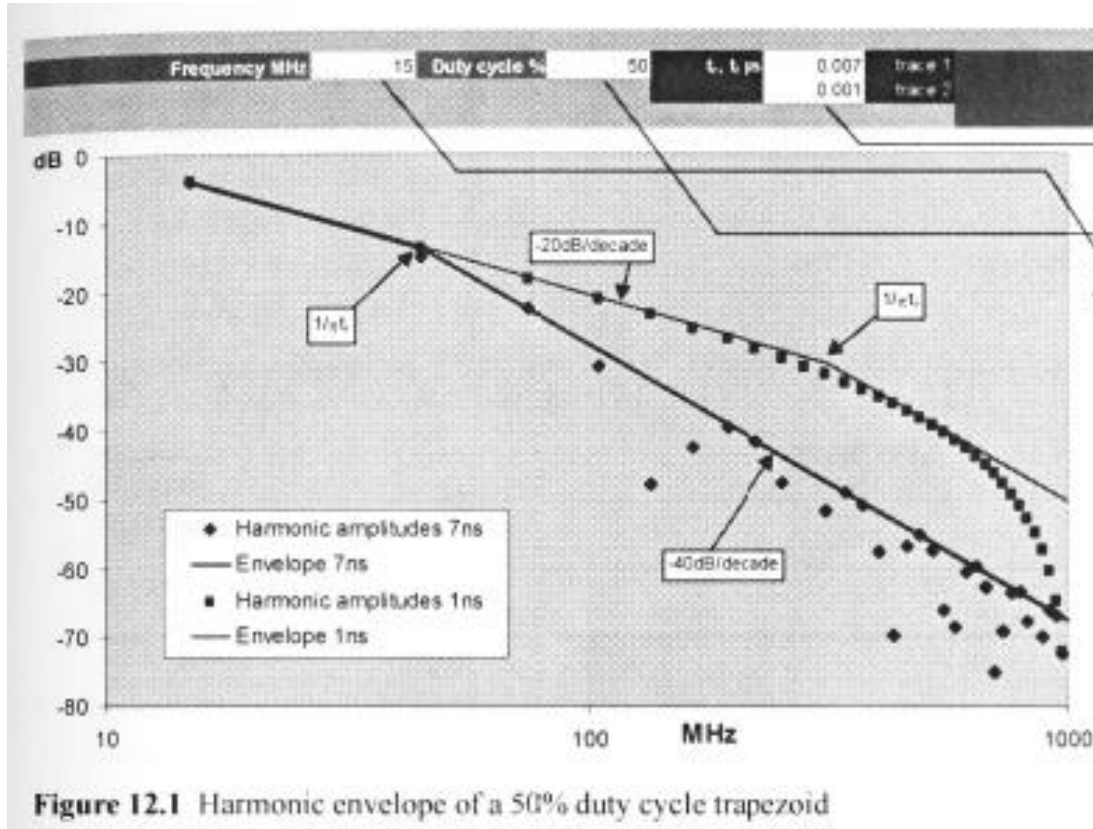
# Föreläsning 7

## IE1332 Utveckling av elektronikprodukter

Kapitel 12 Digital and analogue circuit design

- Kretskonstruktion för EMC
  - Digitala kretsar
  - Analoga kretsar

# Fourierspektrum



$$\frac{1}{\pi t_r}$$

Stigtid  $t_r$

1 ns

7 ns

Slöare kretsar bättre ur EMC-synpunkt!

# Strömspikar vid switchning

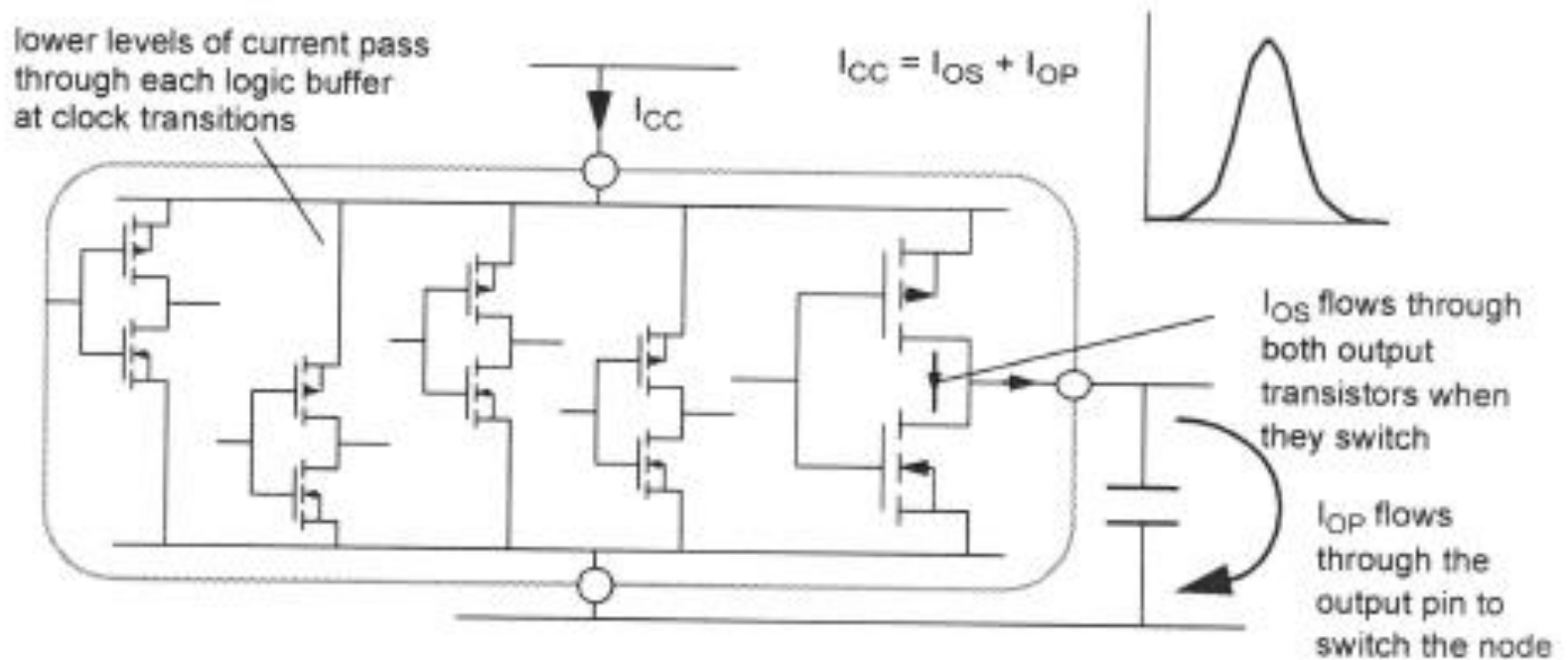


Figure 12.4 Current through the supply pin

# Emission digital trapezoid

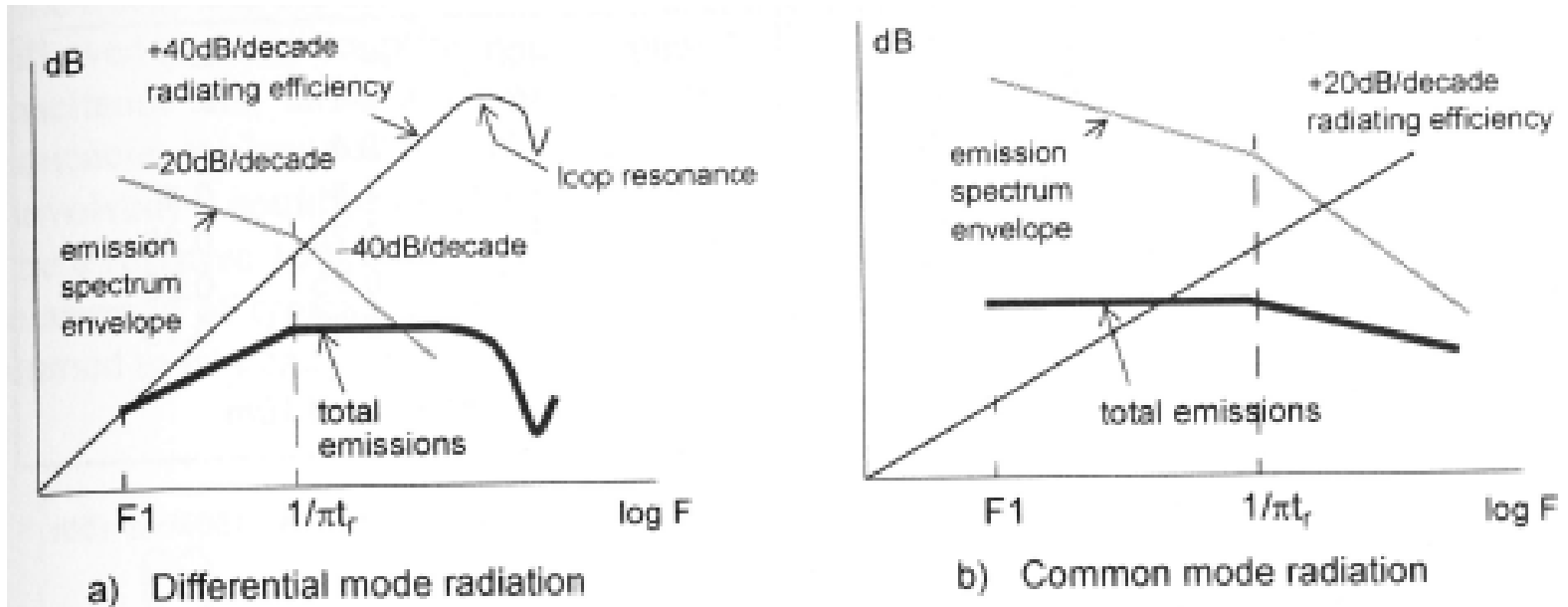


Figure 12.5 Emissions from digital trapezoid waves via different paths

# Differential mode emission, max tillåten loop area

**Table 12.1** Differential mode emission: allowable loop area

Logic family	$t_r/t_f$ ns	$\Delta I$ mA	Loop area $\text{cm}^2$ at clock frequency			
			4MHz	10MHz	30MHz	100MHz
4000B CMOS @ 5V	40	6	1000	400	–	–
74HC	6	20	45	18	6	–
74LS	6	50	18	7.2	2.4	–
74ALS	3.5	50	10	4	1.4	0.4
74AC	3	80	5.5	2.2	0.75	0.25
74F	3	80	5.5	2.2	0.75	0.25
74AS	1.4	120	2	0.8	0.3	0.15

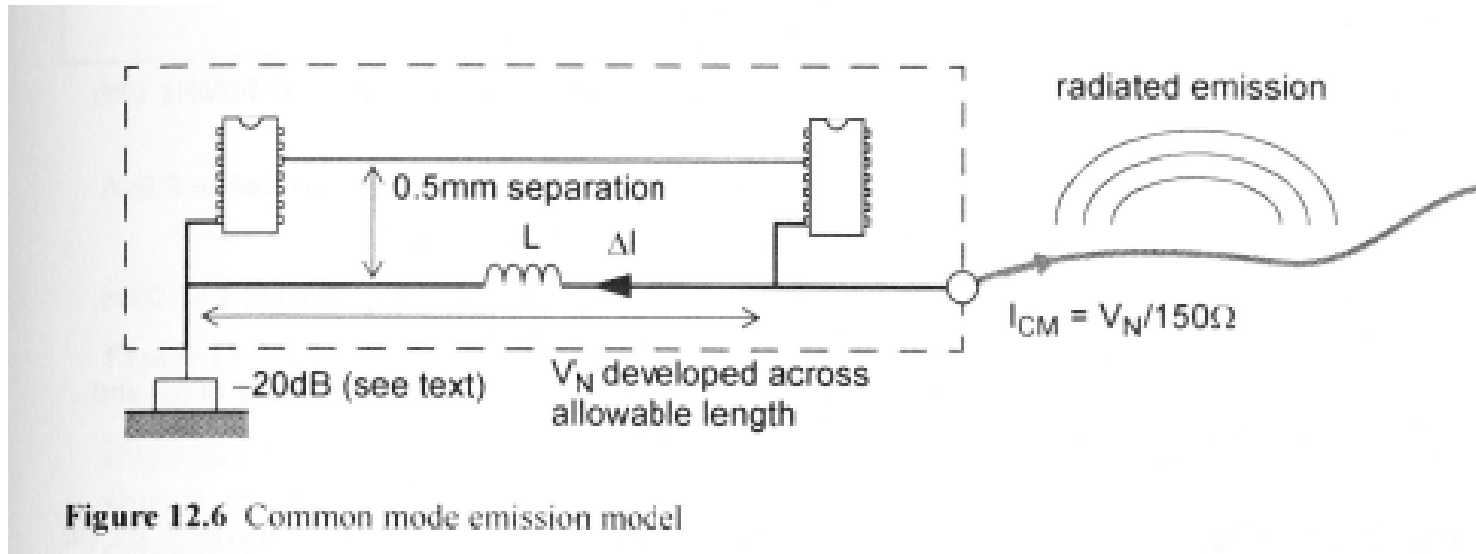
Loop area for 30dB $\mu$ V/m 30MHz–230MHz, 37dB $\mu$ V/m 230–1000MHz at 10m

Working: take 74ALS family with  $F_{\text{clk}} = 30\text{MHz}$  as example. Worst case is at 150MHz (5th harmonic)

Fourier analysis of the source current using section D.7 on page 467 with  $(t + t_r)/T = 0.5$ ,  $T = 33.3\text{ns}$ ,  $t_r = 3.5\text{ns}$  and  $I = 50\text{mA}$  gives  $I_{(5)}$ , the current at the 5th harmonic, as 3.83mA.

From equation (10.12), for a field strength  $E$  of 30dB $\mu$ V/m and  $I_{(5)}$  at 150MHz as above, the allowable loop area  $A$  is **1.395cm<sup>2</sup>** (rounded to 1.4 in the table).

# Common mode emission



- ensuring that logic currents do not flow between the ground reference point and the point of connection to external cables;
- filtering all cable interfaces to a “clean” ground as discussed in section 11.2.3.1;
- screening cables with the screen connection made to a “clean” ground;
- minimizing ground noise voltages by using low inductance ground layout, preferably involving a ground plane.

# Common mode, maximalt tillåten ledningslängd

Table 12.2 Common mode emission: allowable track length

Logic family	$t_r/t_f$ ns	$\Delta I$ mA	Track length cm at clock frequency			
			4MHz	10MHz	30MHz	100MHz
4000B CMOS @ 5V	40	6	180	75	—	—
74HC	6	20	8.5	3.2	1	—
74LS	6	50	3.25	1.3	0.45	—
74ALS	3.5	50	1.9	0.75	0.25	0.08
74AC	3	80	1.0	0.4	0.14	0.05
74F	3	80	1.0	0.4	0.14	0.05
74AS	1.4	120	0.4	0.15	0.05	—

Allowable track length for 30dB $\mu$ V/m 30MHz–230MHz, 37dB $\mu$ V/m 230–1000MHz at 10m; cable length = 1m; layout: parallel 0.5mm tracks 0.5mm apart (2.8nH/cm)

Working: take 74HC family with  $F_{clk} = 10\text{MHz}$  as an example. Worst case is at 90MHz (9th harmonic).

From equation (10.13), for a field strength  $E$  of 30dB $\mu$ V/m and 1m cable length,  $I_{CM}$  must be 2.8 $\mu$ A.

From  $V_N = I_{CM} \cdot 150$  and including 20dB coupling attenuation,  $V_N = 4.18\text{mV}$ .

Fourier analysis of the source current using section D.7 on page 467 with  $(t + t_r)/T = 0.5$ ,  $T = 100\text{ns}$ ,  $t_r = 6\text{ns}$  and  $I = 20\text{mA}$  gives  $I_{(9)}$ , the current at the 9th harmonic, as 0.826mA.

Now from  $L = V_N/2 \cdot \pi \cdot f \cdot I_{(9)}$ , the allowable inductance across which  $V_N$  will be developed at  $I_{(9)}$  and 90MHz is 8.95nH which at 2.8nH/cm gives **3.19cm** allowed.

# Typisk emission, 40 MHz klockoscillator

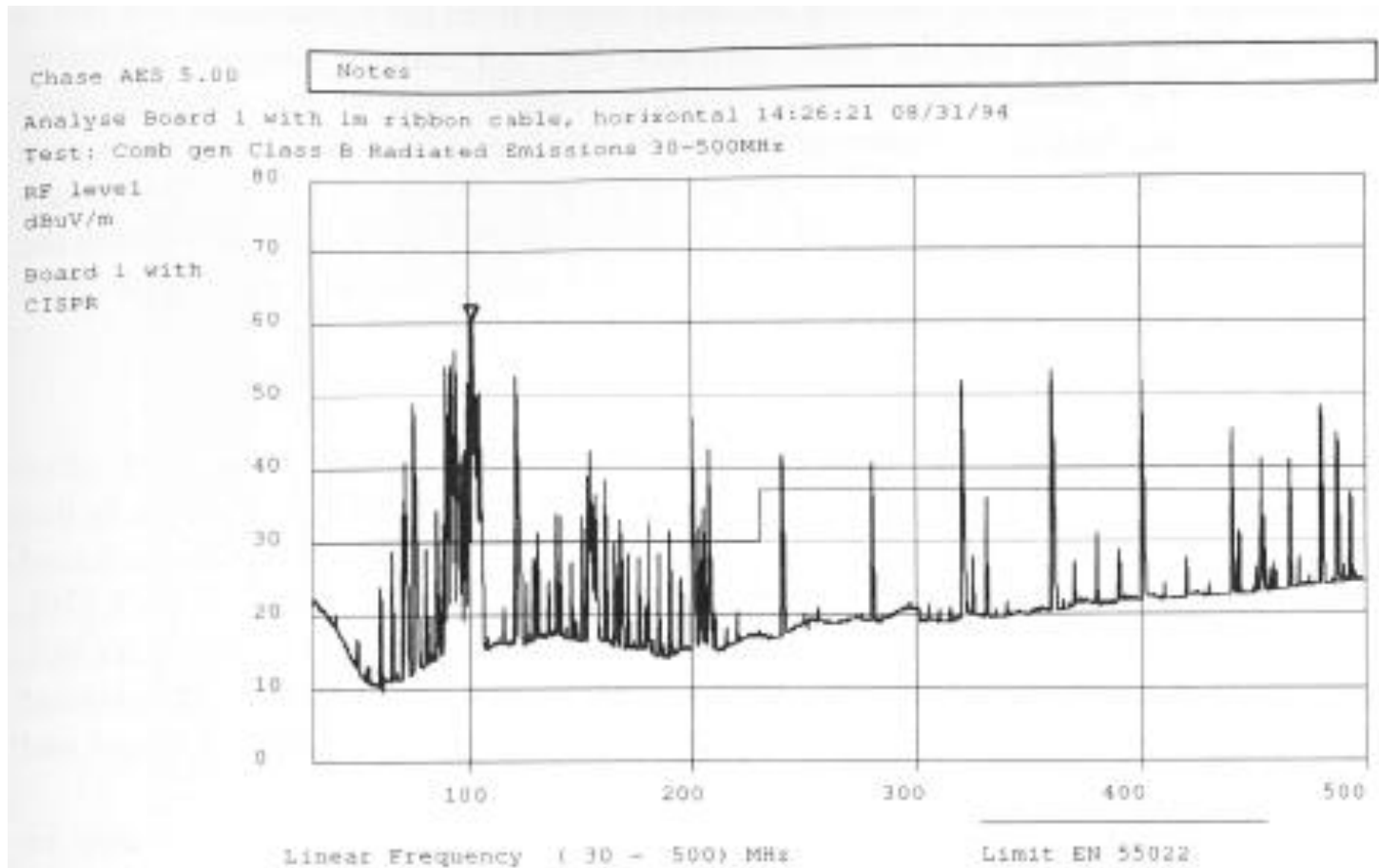


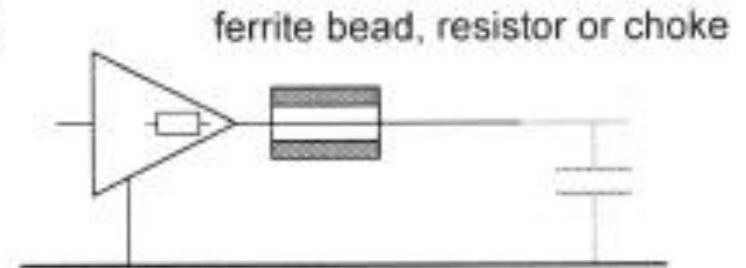
Figure 12.7 Typical emissions plot showing clock harmonics



# Slöa ned flankerna på klockan!



a) parallel capacitance (not recommended)



b) series impedance

**Figure 12.8** Controlling the clock edges

[Ferrite bead](#)

# Layout av bakplan

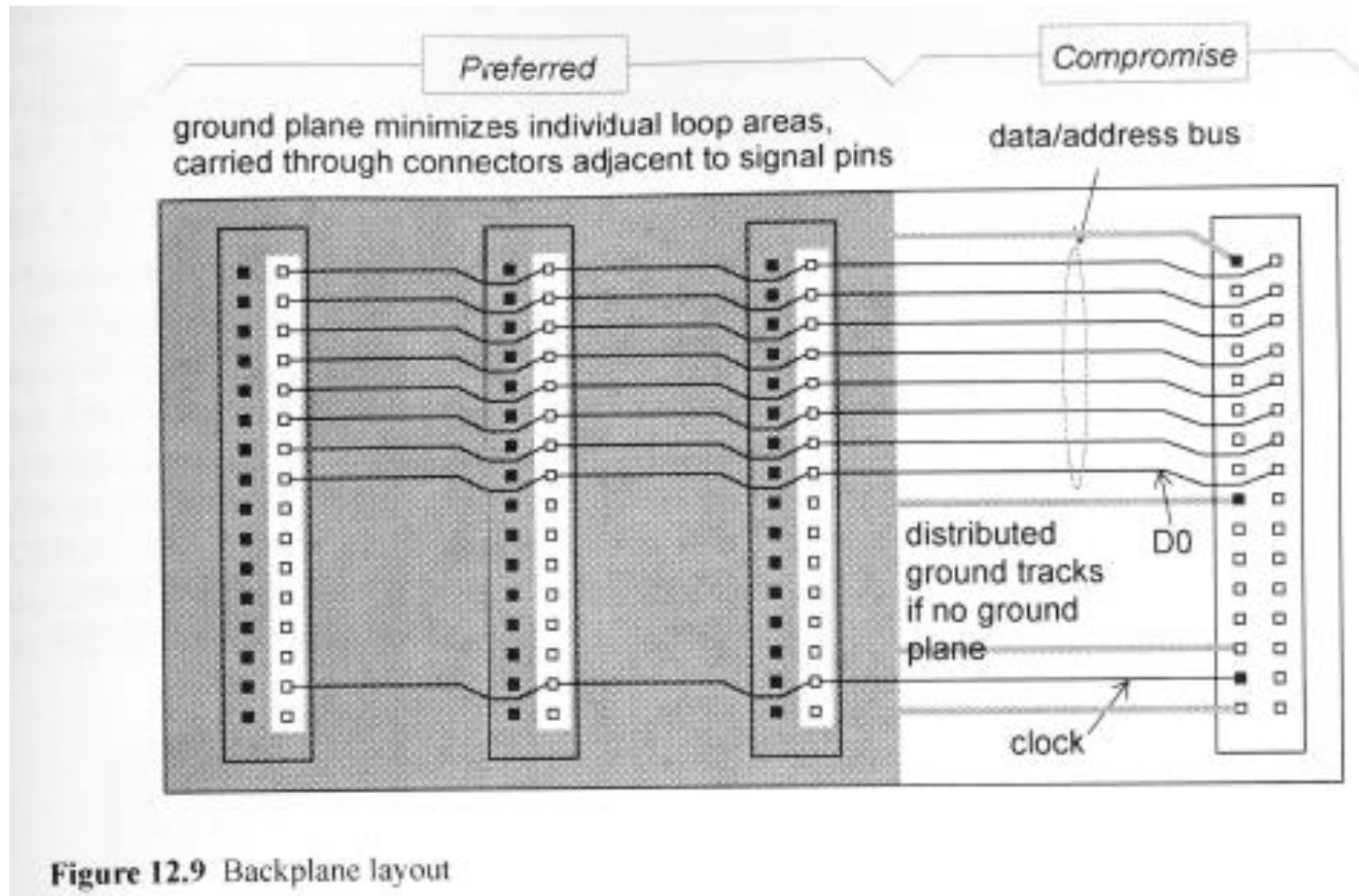
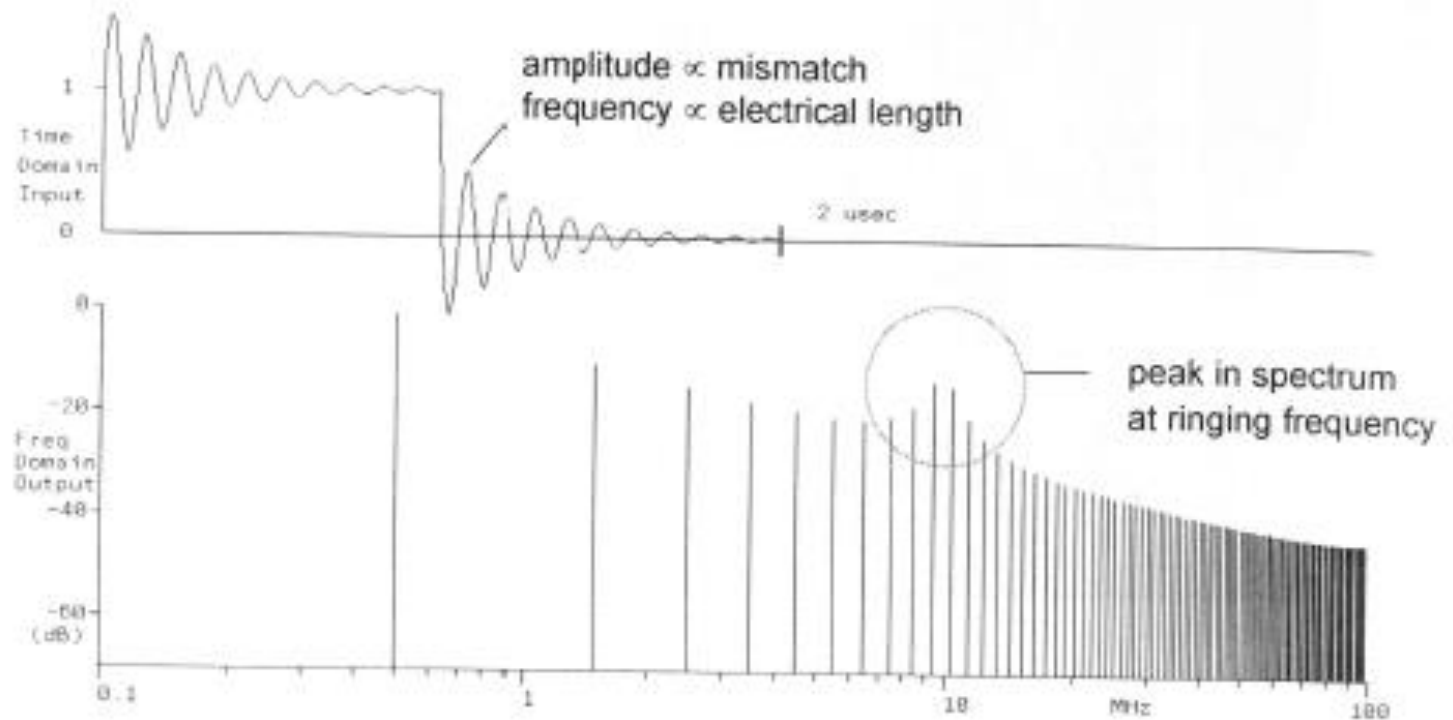


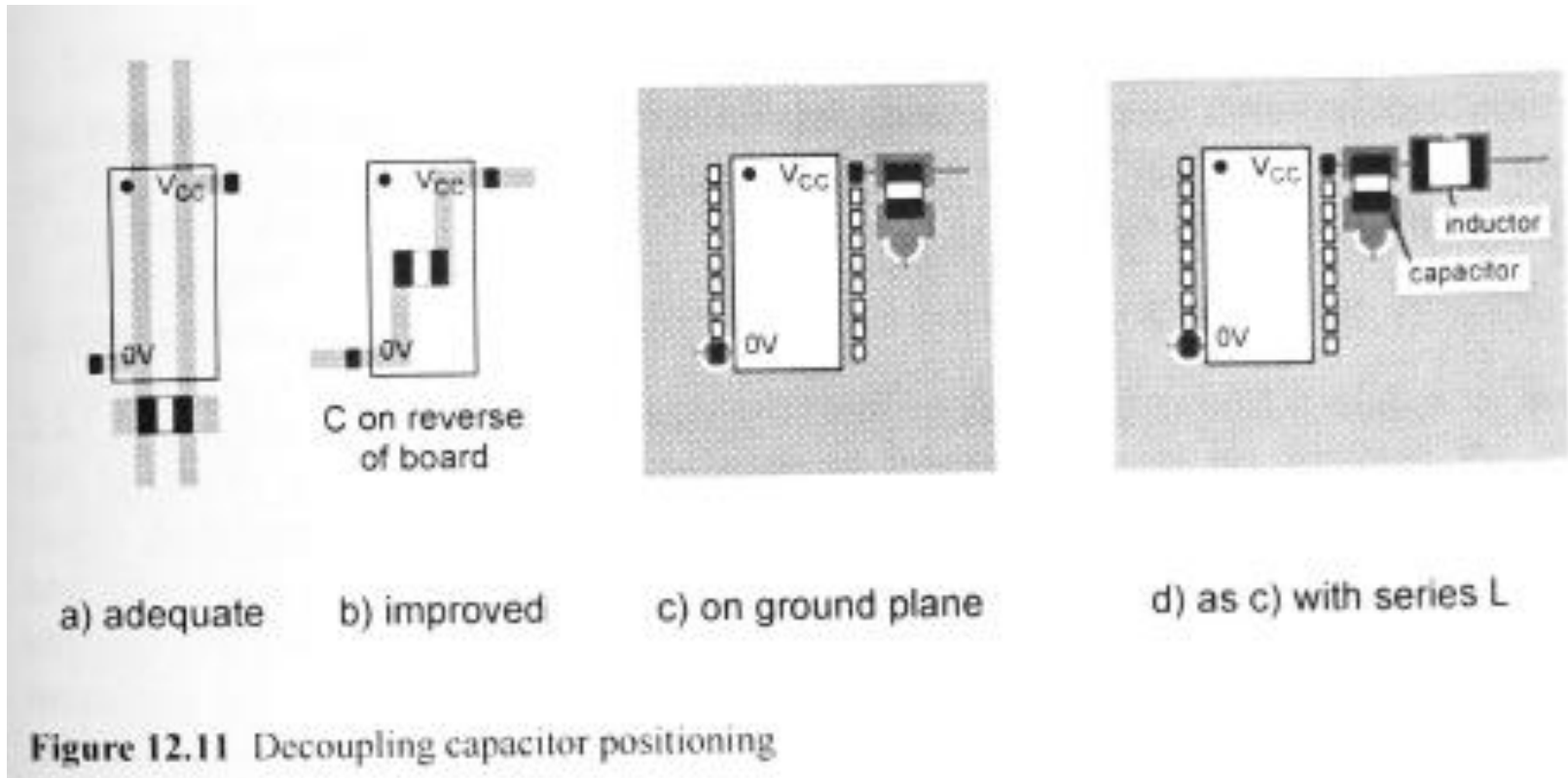
Figure 12.9 Backplane layout

# Ringning pga dåligt anpassad ledning

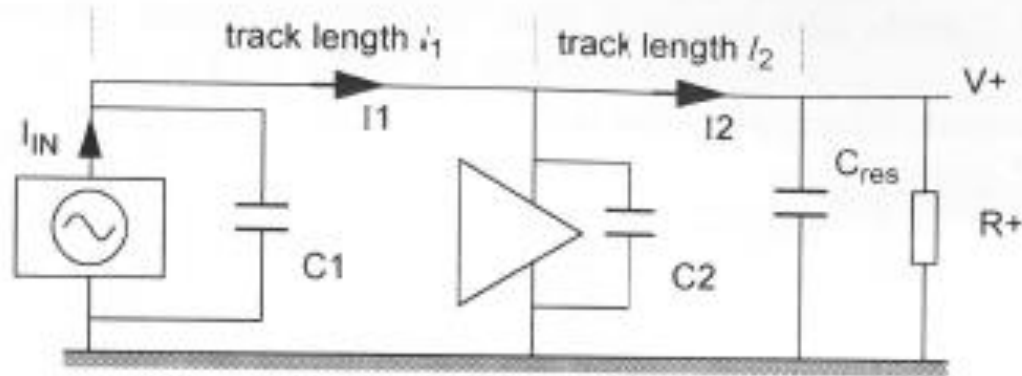


**Figure 12.10** Ringing due to a mismatched transmission line

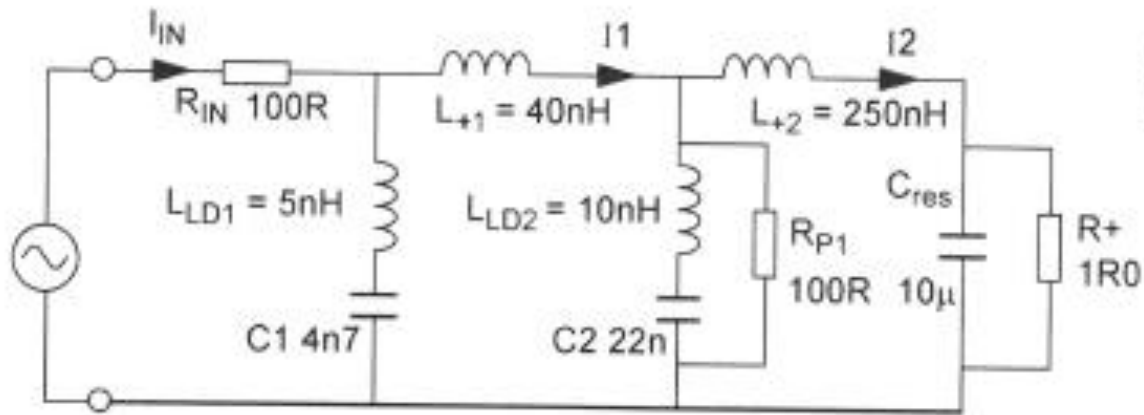
# Placering av avkopplingskondensator



# Analys av avkoppling, bild 1



Model circuit



Equivalent circuit

# Analys av avkoppling, bild 2

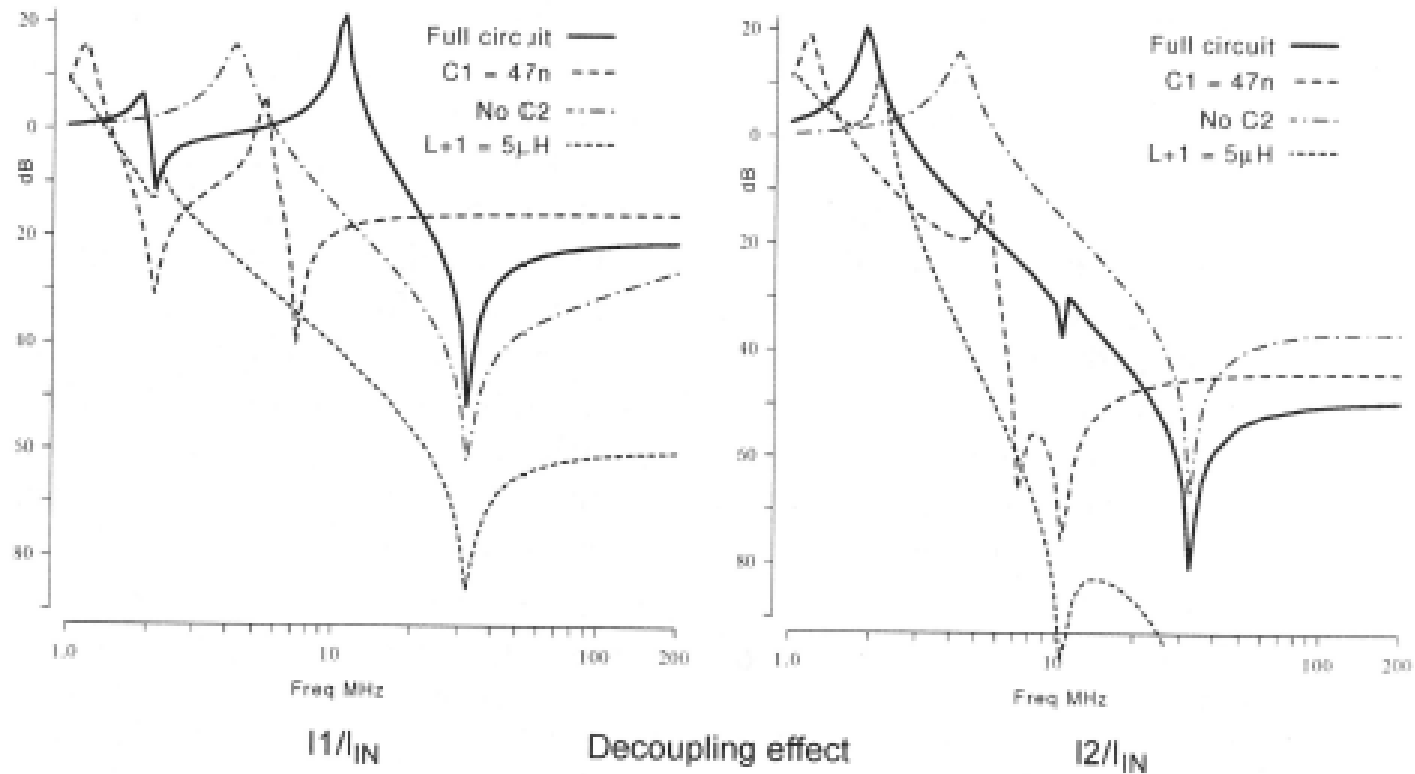
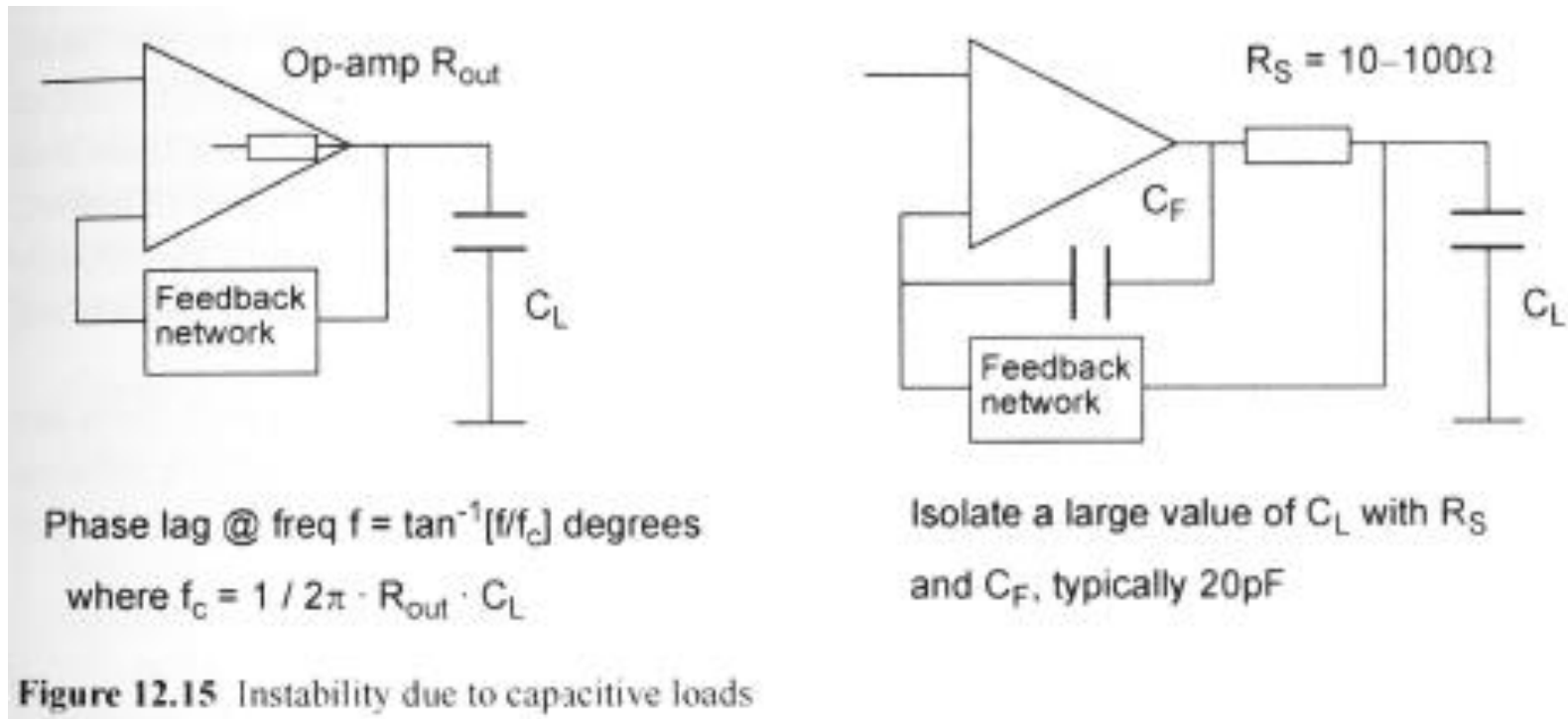


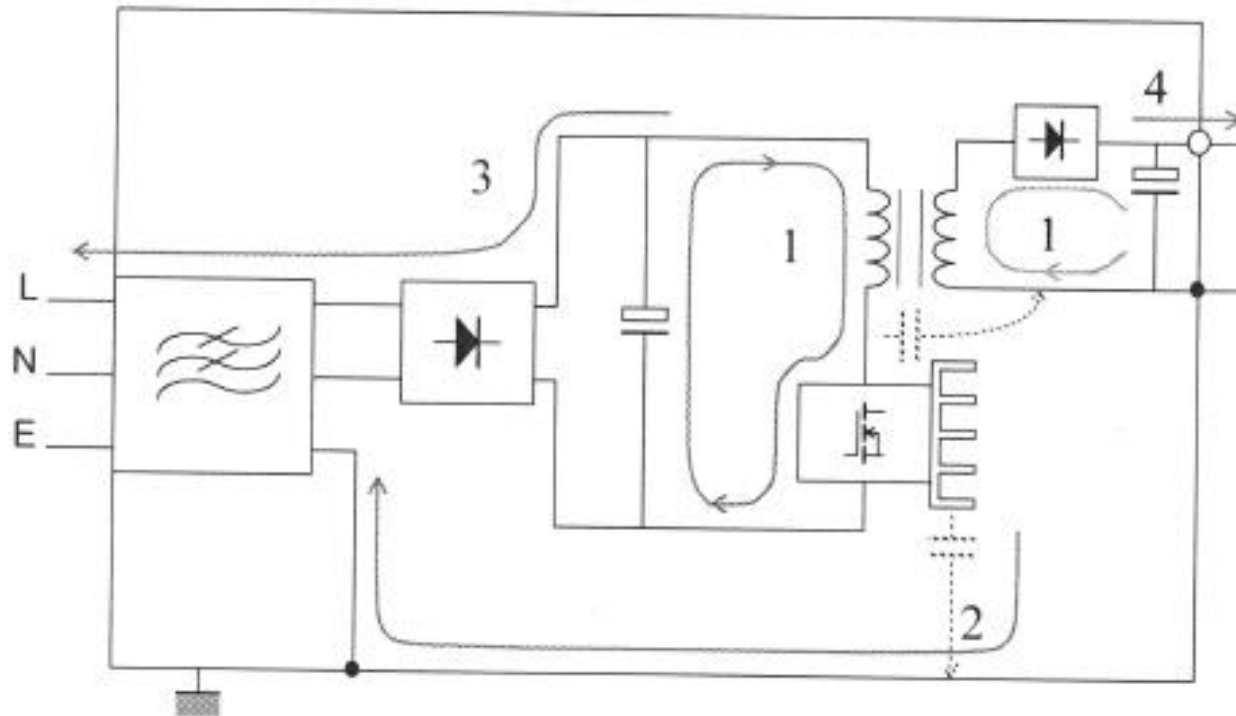
Figure 12.13 Analysing the decoupling equivalent circuit

# Emission från analoga kretsar

## Självsvängning pga kapacitiv last



# Switchat nätaggregat, hög di/dt



- 1: H-field radiation from high di/dt loop
- 2: capacitive coupling of E-field radiation from high dv/dt node to earth
- 3: differential mode current conducted through DC link
- 4: conducted and/or radiated on output

Figure 12.16 Switching supply emission paths



# Kapacitiv koppling, hög $dv/dt$

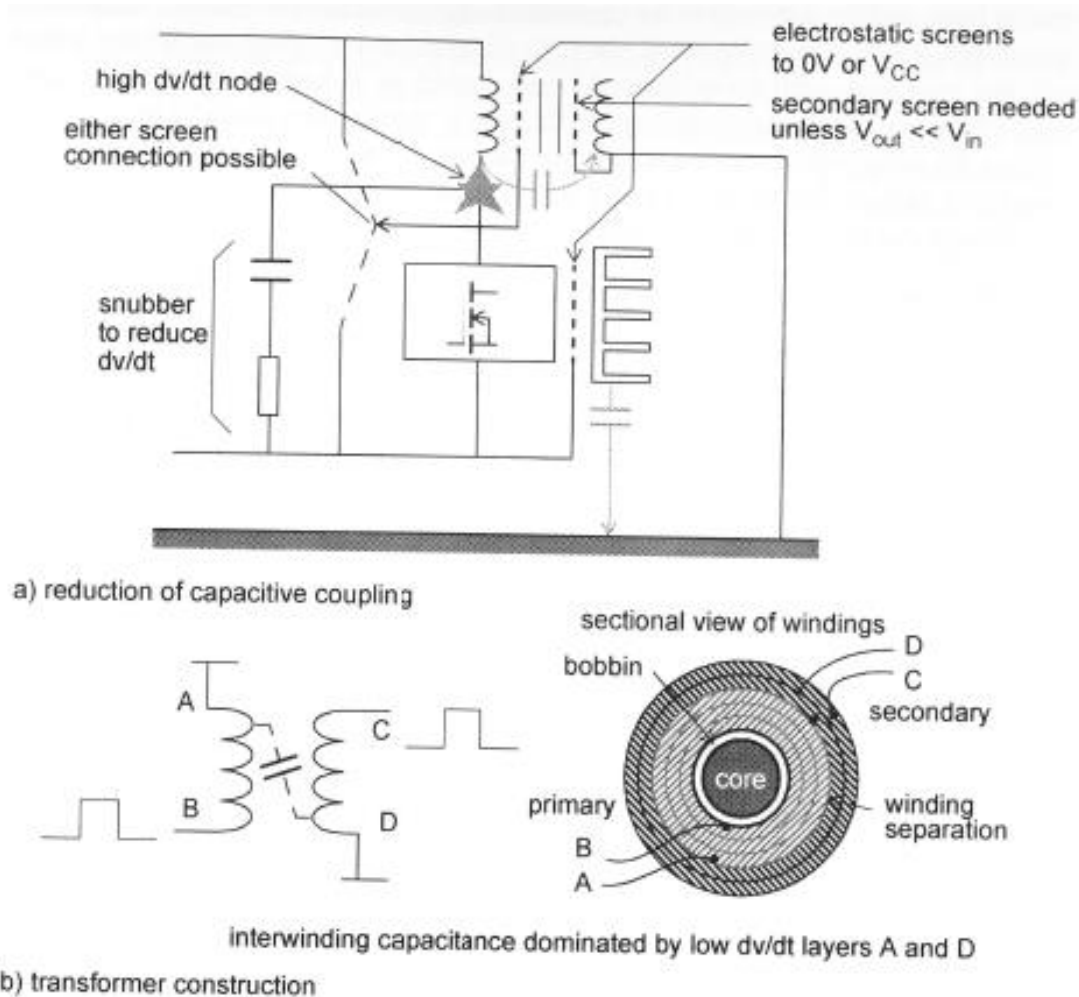


Figure 12.17 Common mode capacitive coupling

# Design för immunitet

- Digitala kretsar
  - Vad kan hända?
  - Hur minska risken?

# Common mode transient från nätet

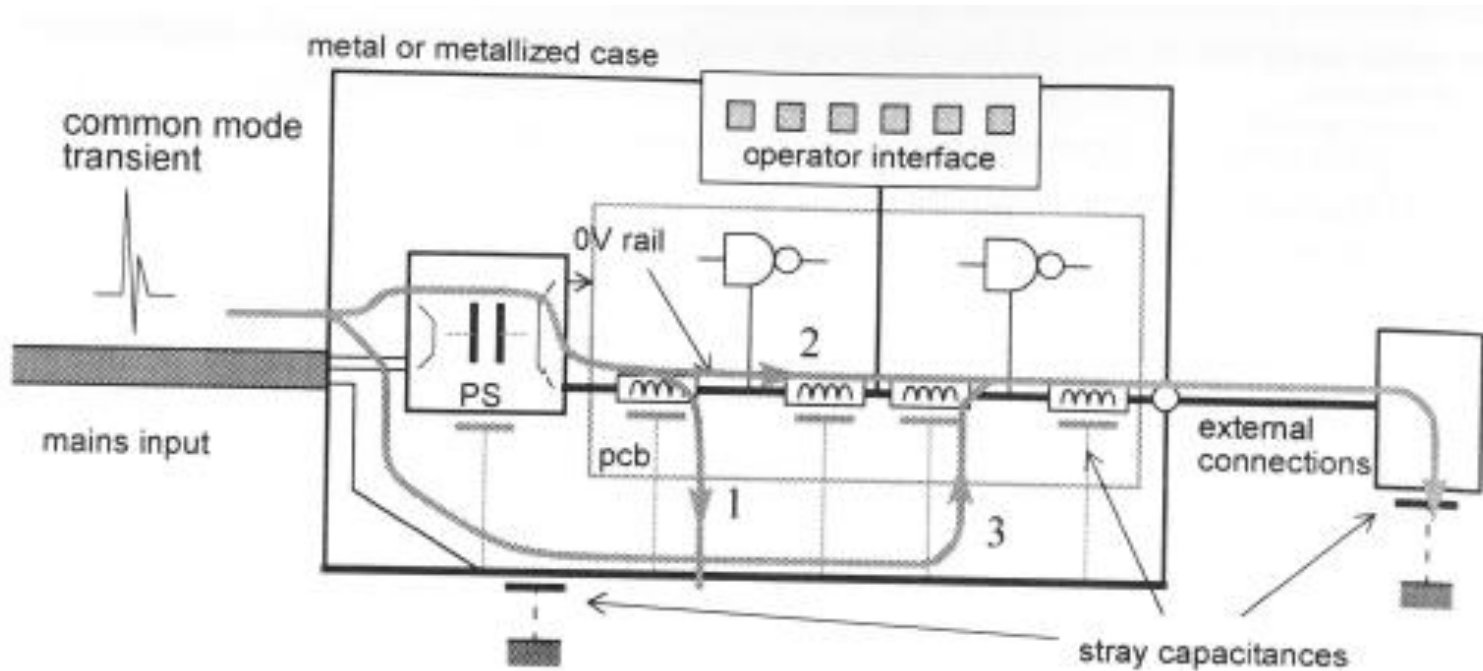
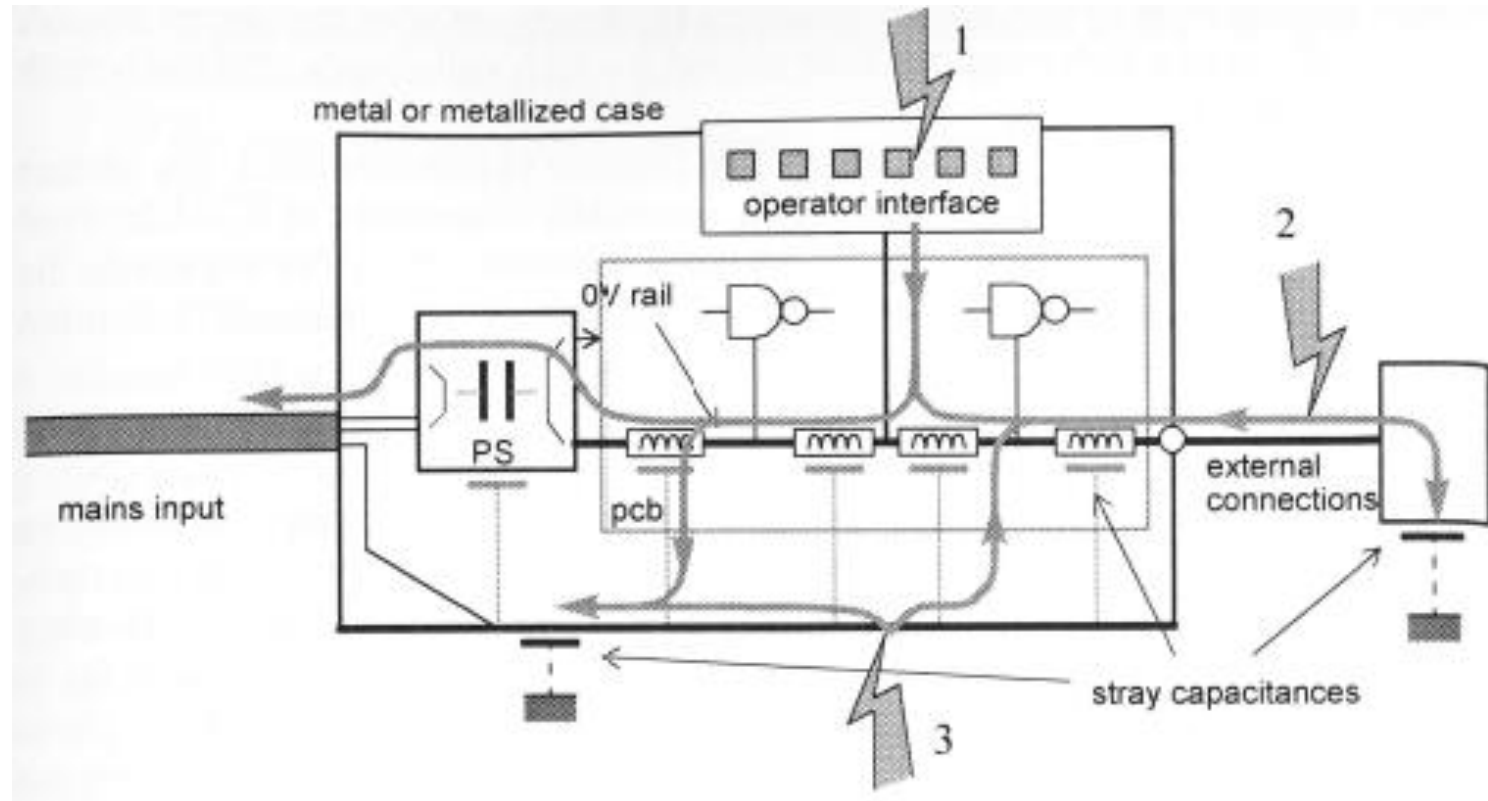


Figure 12.21 Representative high frequency equivalent circuit: transients

# ESD urladdning mot metallhöljet eller via användargränssnitt



# Transient- och ESD-skydd

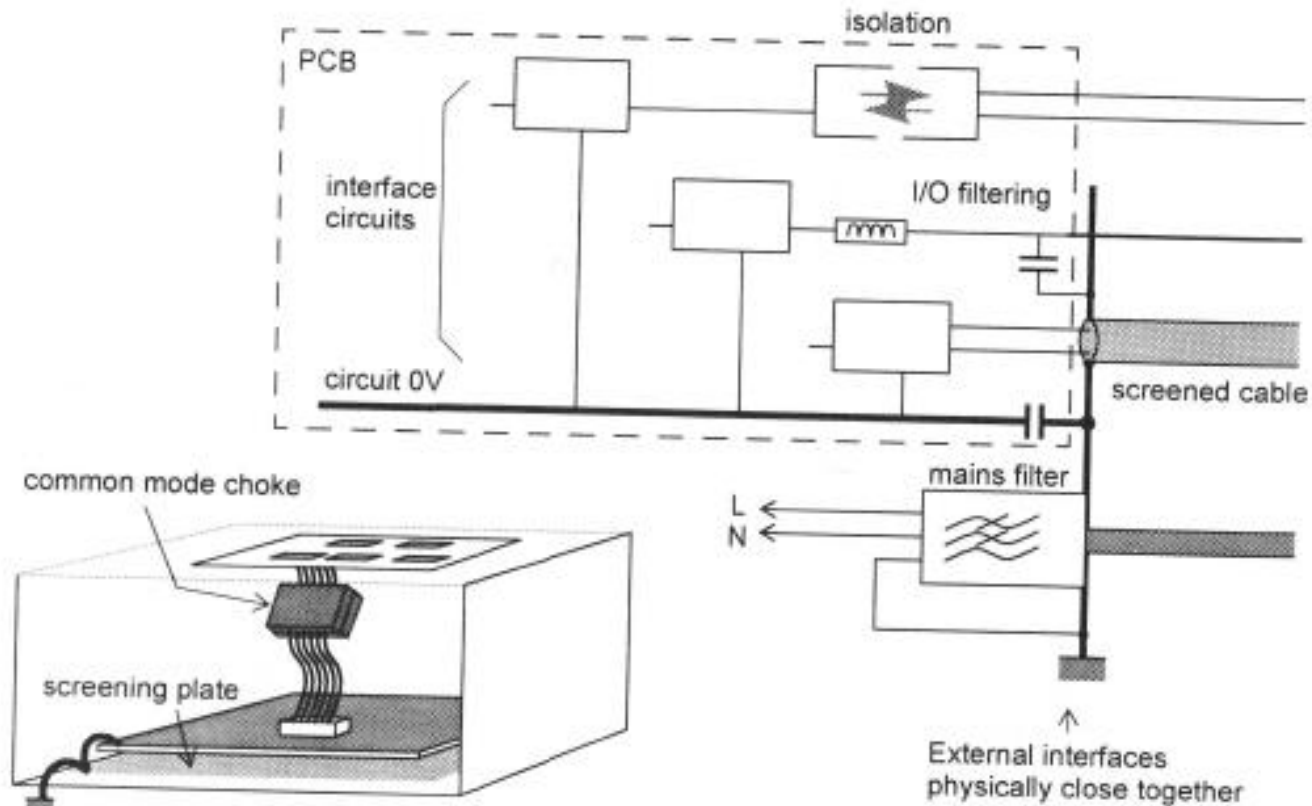
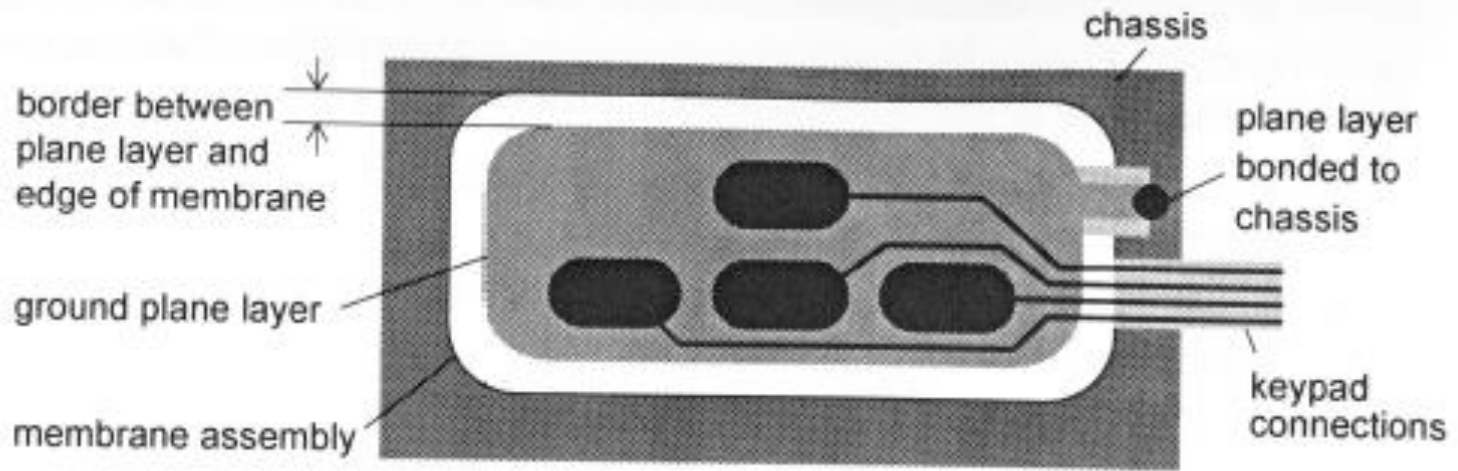


Figure 12.23 Transient and ESD protection

# Jordplan till tangentbord



**Figure 12.24** Ground plane on a membrane keypad

# ESD-skydd

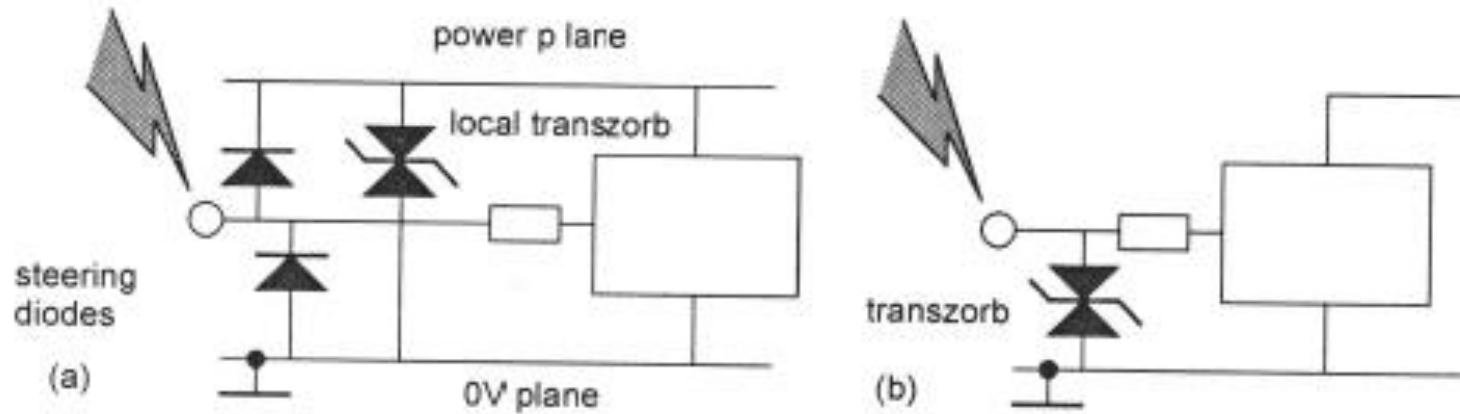
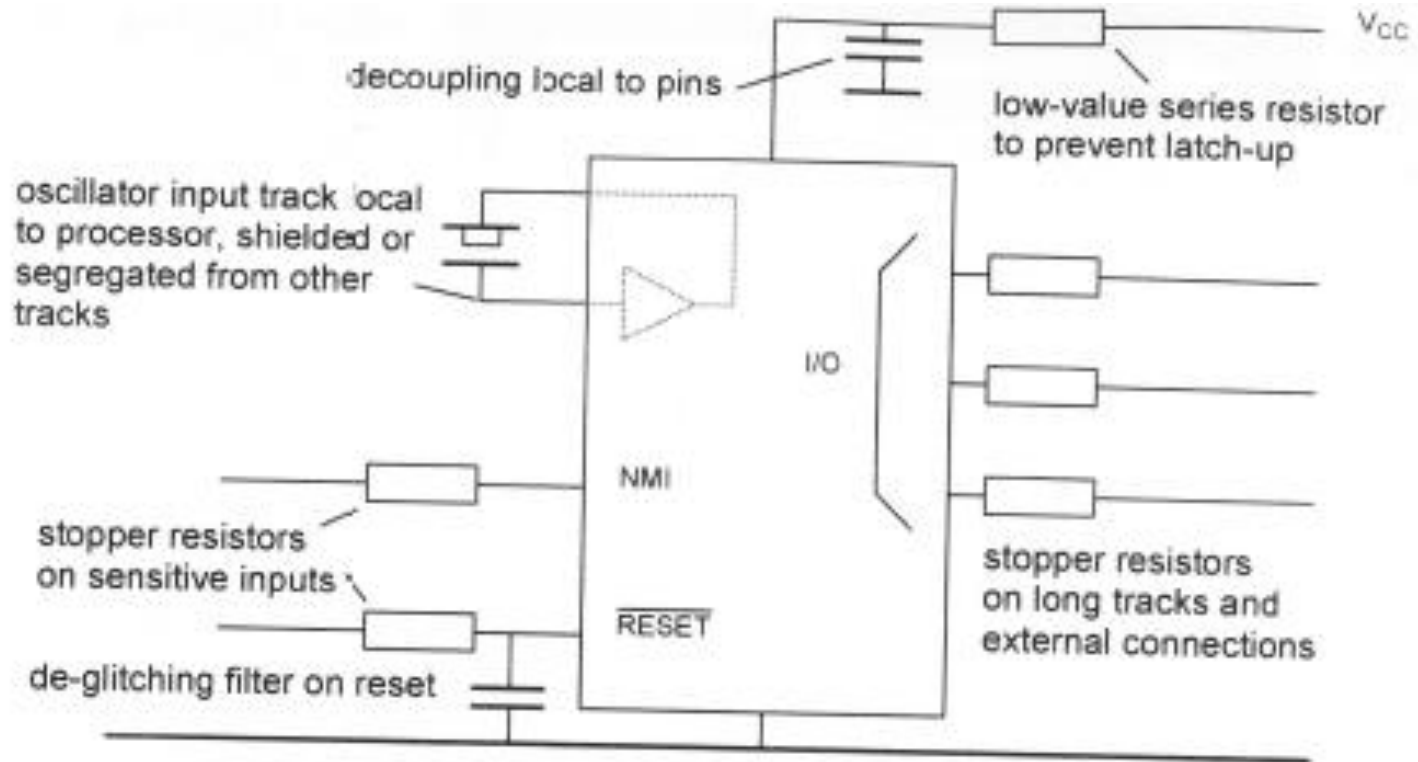


Figure 12.25 ESD interface protection

# Immunitet microcontroller



**Figure 12.26** Immunity precautions around microcontrollers



# Watchdog

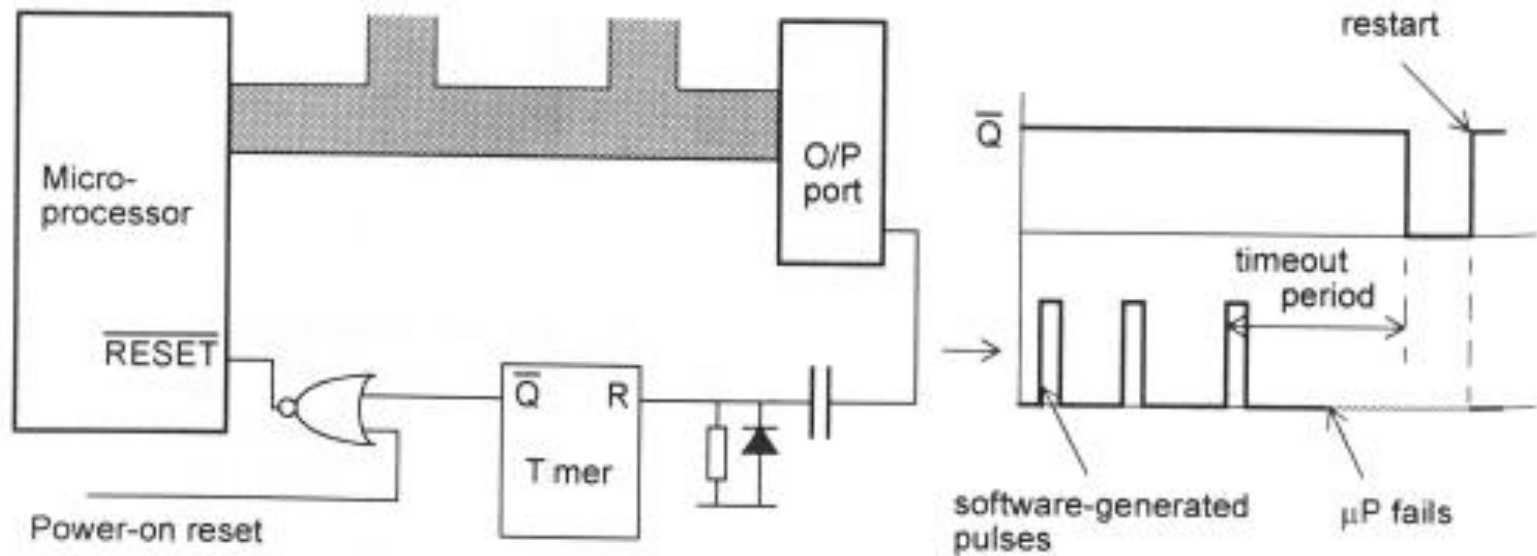
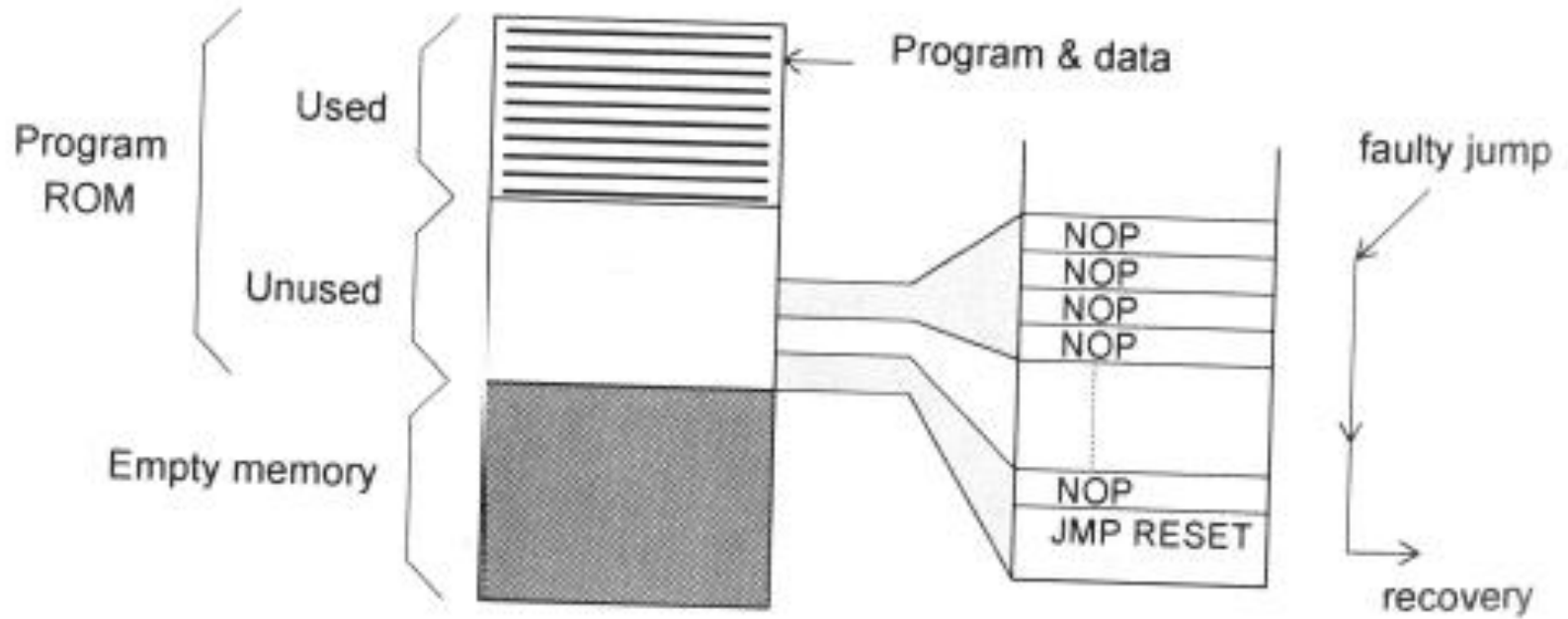


Figure 12.32 Watchdog operation

# NOP



**Figure 12.36** Protecting unused program memory with NOPs

# Design för immunitet

- Analoga kretsar
  - Vad kan hända?
  - Hur minska risken?

# Immunitet analoga kretsar

## Analogue immunity principles

- minimize circuit bandwidth
- maximize signal levels
- ensure a good circuit stability margin
- use balanced signal configurations
- isolate particularly susceptible paths

# RF kan påverka lågfrekvenskresor

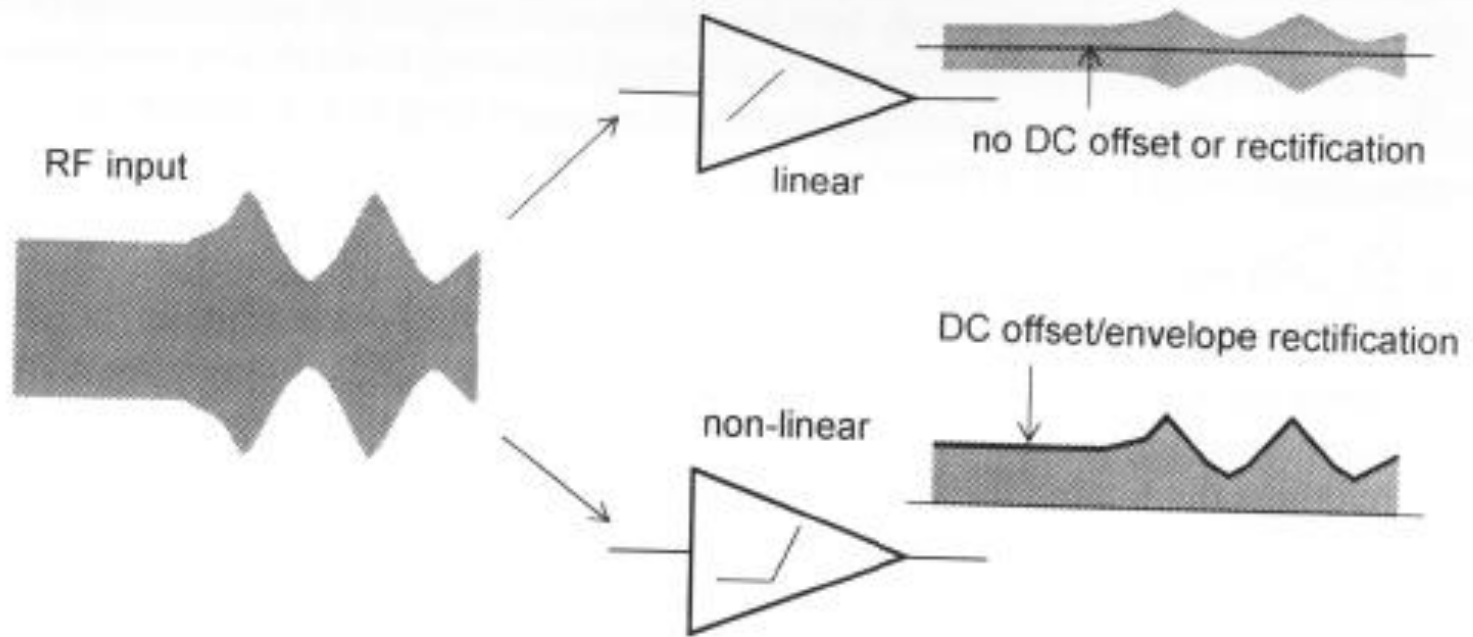
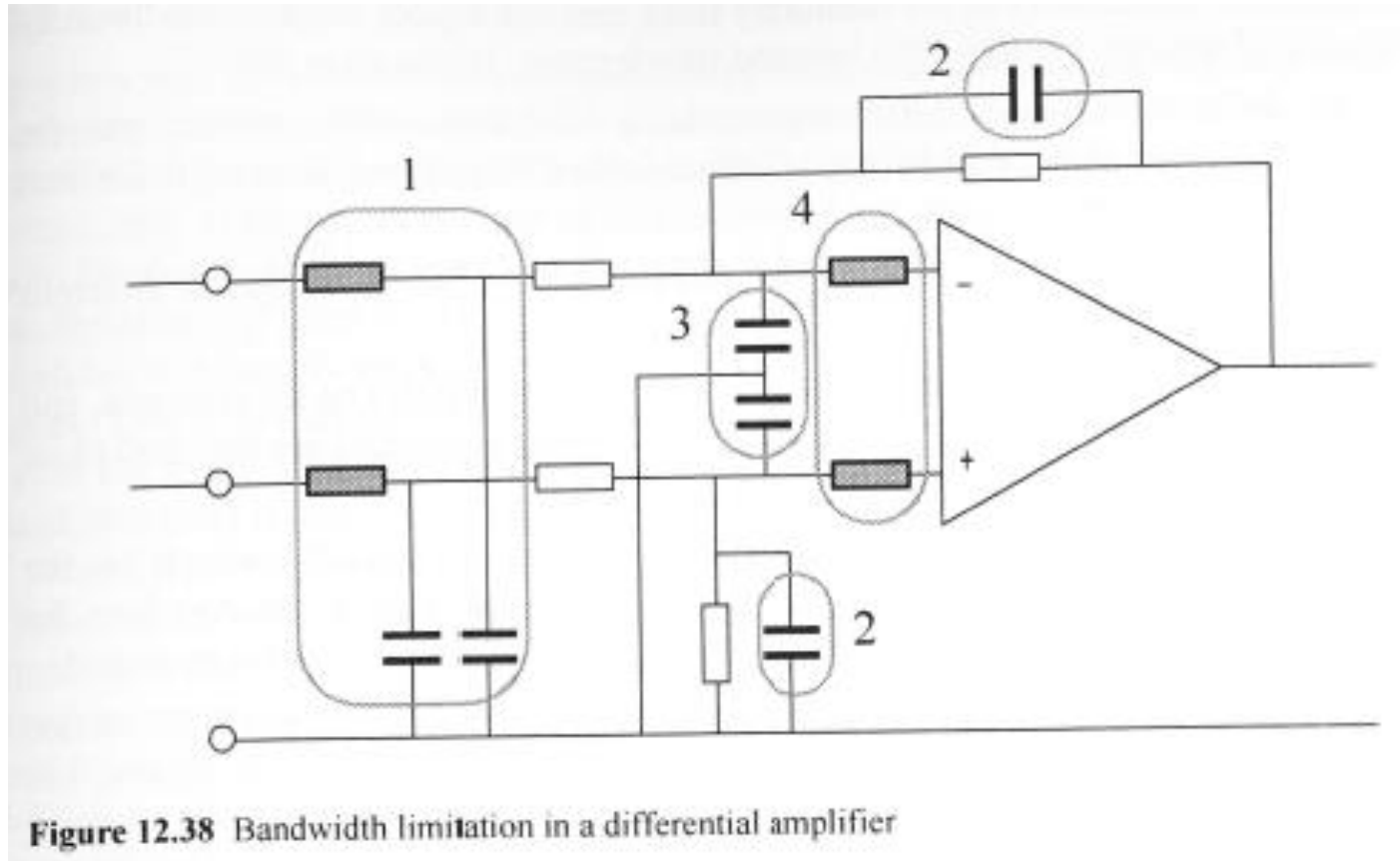


Figure 12.37 RF demodulation by non-linear circuits

# Begräns bandbredden



# Isolera signaler

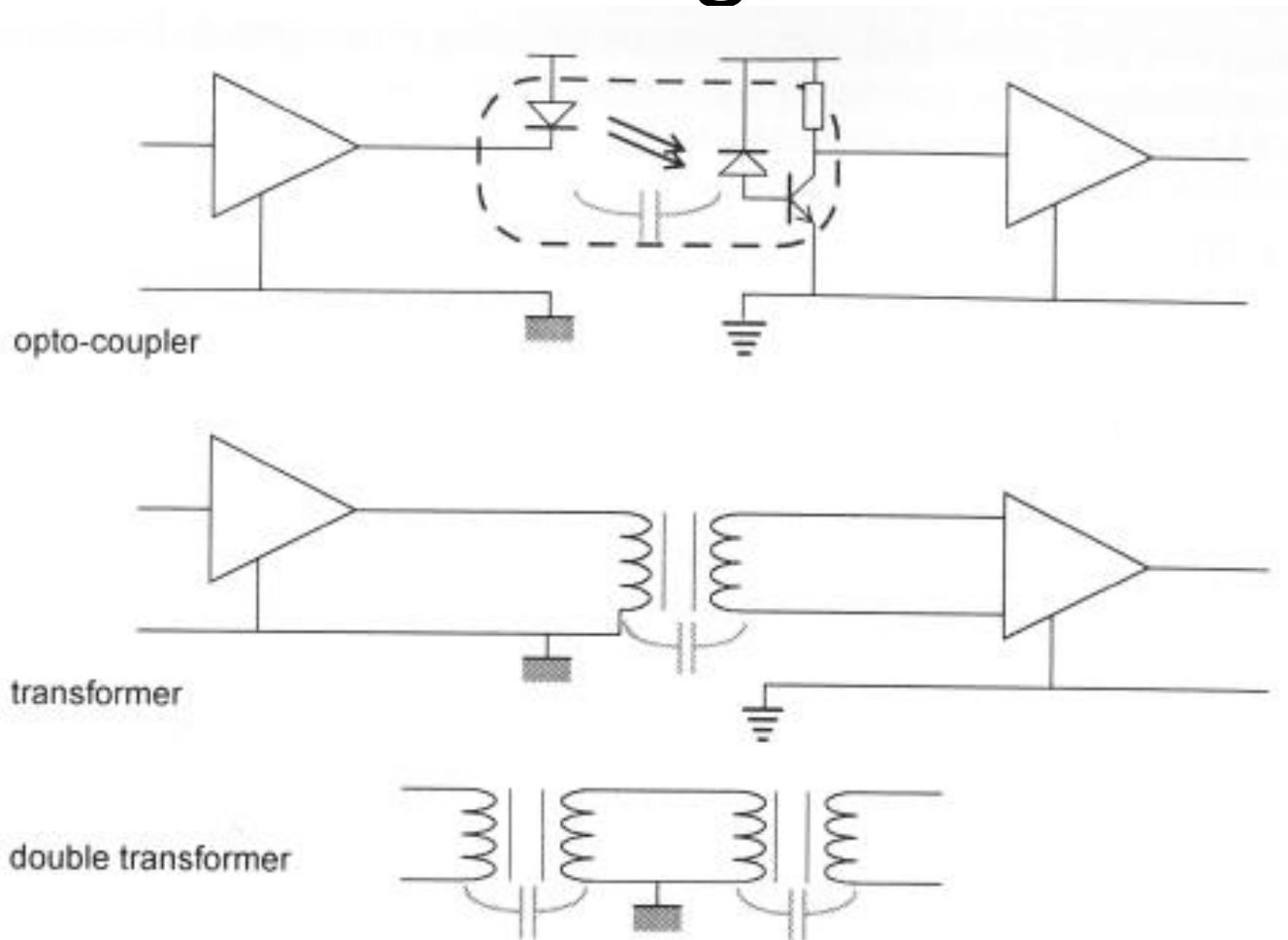


Figure 12.42 Signal isolation