

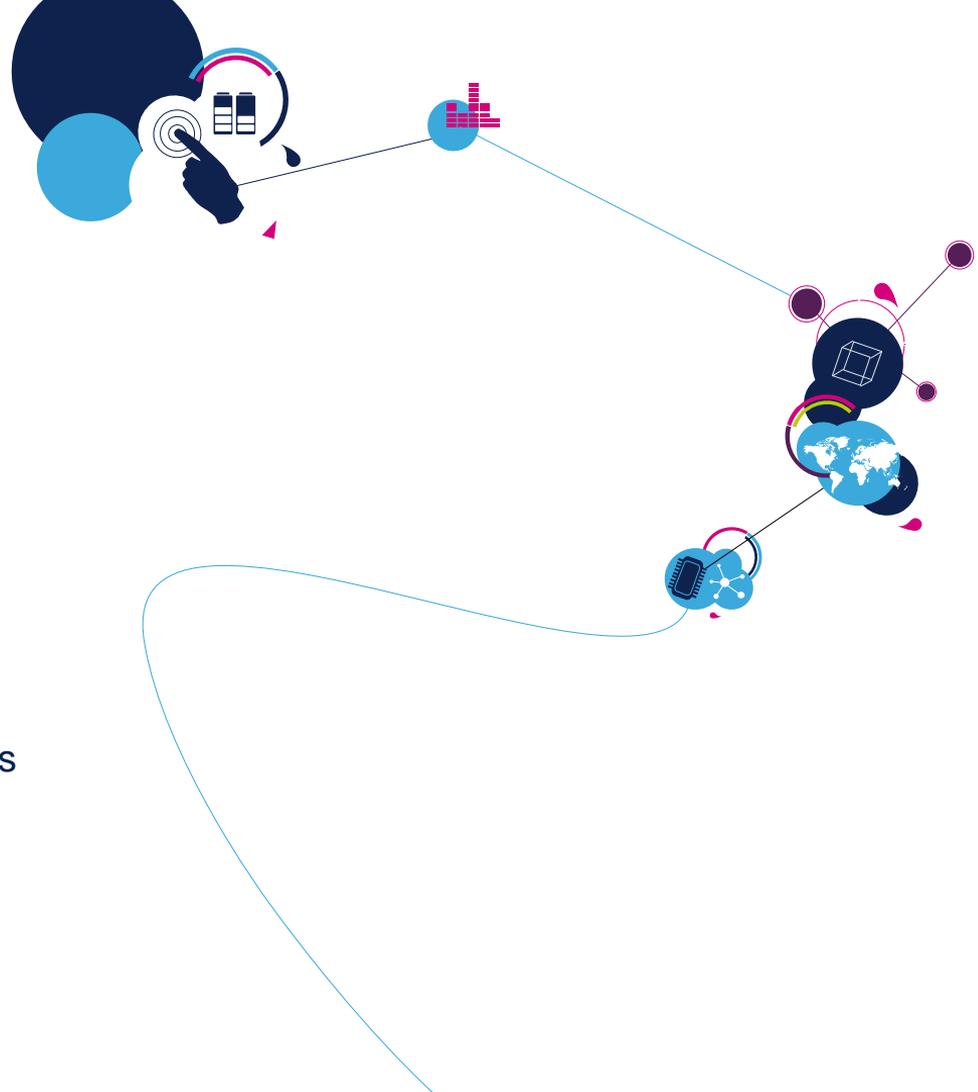
Microcontrollers

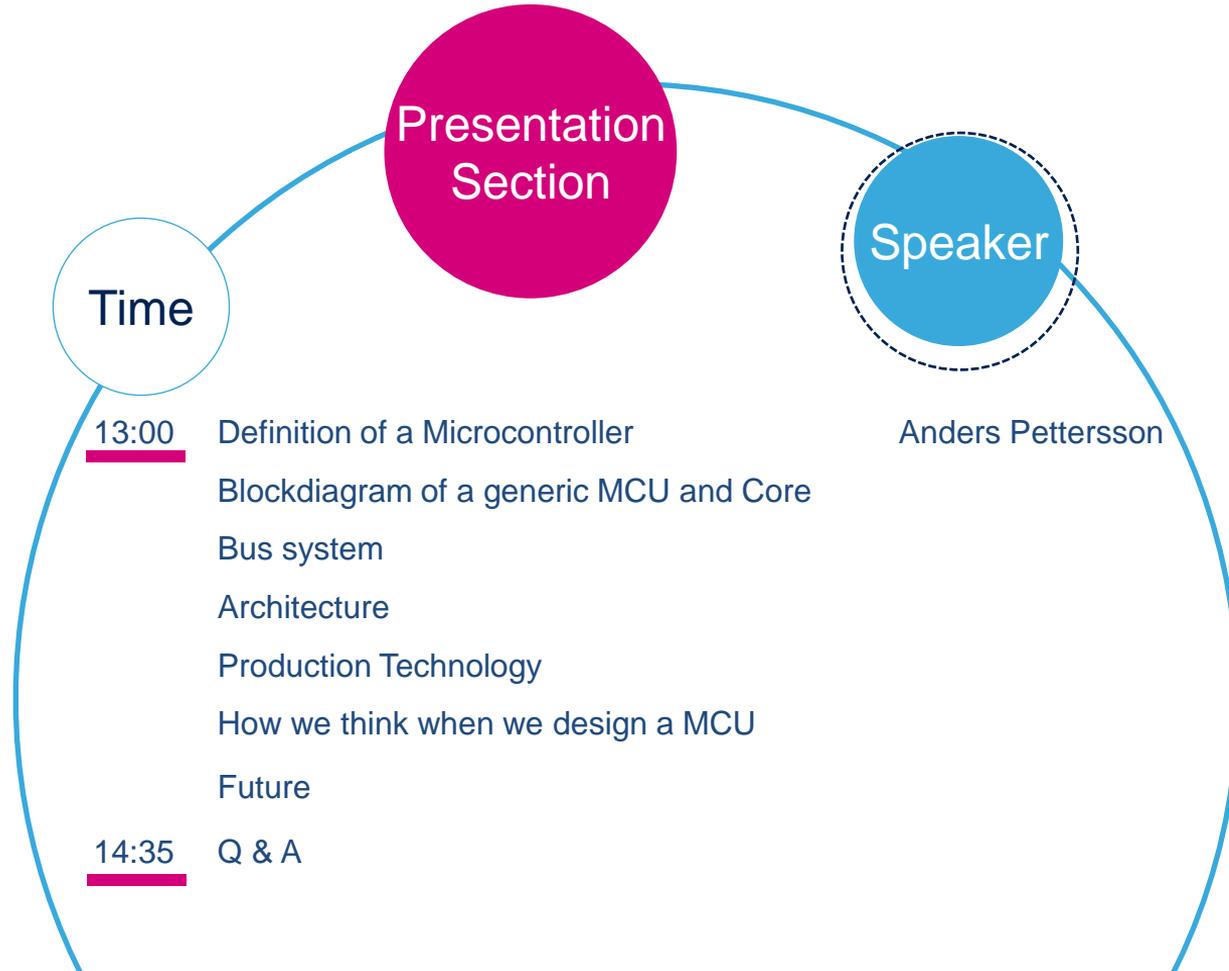
-Definition, Basics and Trends

Anders Pettersson

Technical Marketing Manager Microcontrollers

Nordic and Baltic





After the session you should have learnt..

- Know the difference between a MCU and a MPU and a CPU.
- Differences between a 8 bit and 32 bit MCU.
- Differences between Risc and Cisc architecture
- Differences between Harvard and Von Neuman Architecture
- Temporary production technologies



Definition of a Microcontroller

Definition of a Microcontroller

- What is the Definition of a Microcontroller?
- There is no absolute definition...

A **microcontroller** (sometimes abbreviated μC , uC or **MCU**) is a small computer on a single **integrated circuit** containing a processor core, memory, and programmable **input/output peripherals**. Program memory in the form of **NOR flash** or **OTP ROM** is also often included on chip, as well as a typically small amount of **RAM**. Microcontrollers are designed for embedded applications, in contrast to the **microprocessors** used in **personal computers** or other general purpose applications.

....from Wikipedia



Architecture

Cisc and Risc

CISC

- Emphasis on HW
- Includes Multi-clock complex instructions
- Memory-to-memory: "LOAD" and "STORE" incorporated in instructions
- Small code sizes, high cycles per second
- Transistors used for storing complex instructions

RISC

- Emphasis on SW
- Single-clock, reduced instructions only
- Register-to-register: "LOAD" and "STORE" and independent from instructions
- Low cycles per second, larger code size
- Spends more transistors on memory registers

Example: Multiply (MULT) , considered as a complex instruction

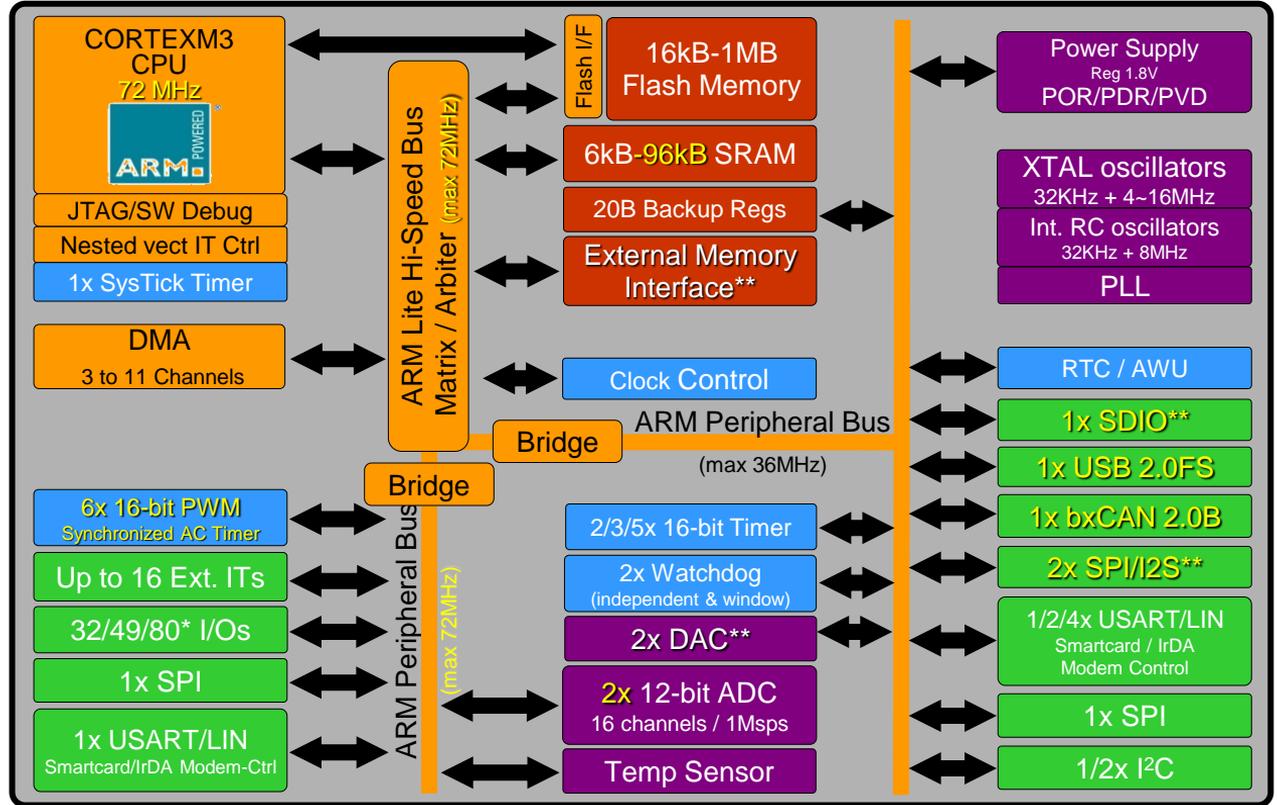
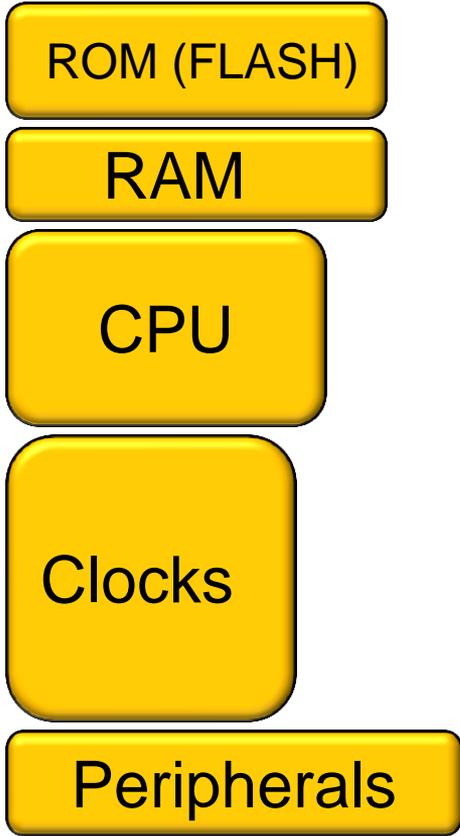
CISC: MULT 2:3, 5:2

RISC: LOAD A, 2:3
LOAD B, 5:2
PROD A, B
STORE 2:3, A



Block diagram and the Core

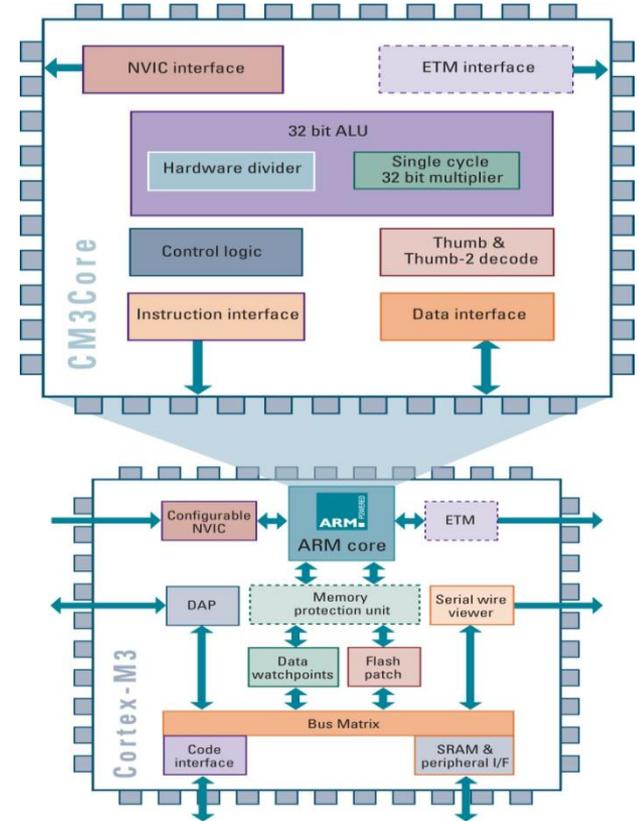
Essential block diagram of a MCU



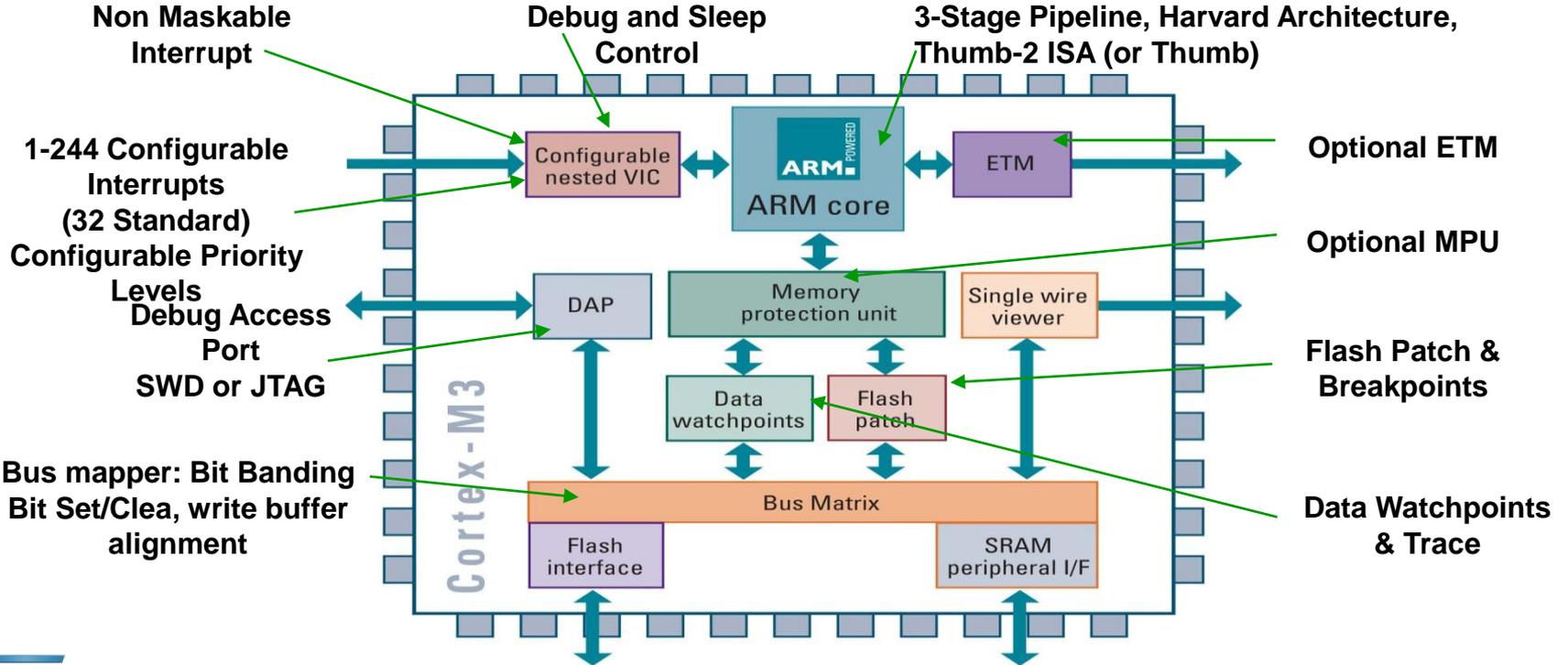
Cortex-M3 Microprocessor

12

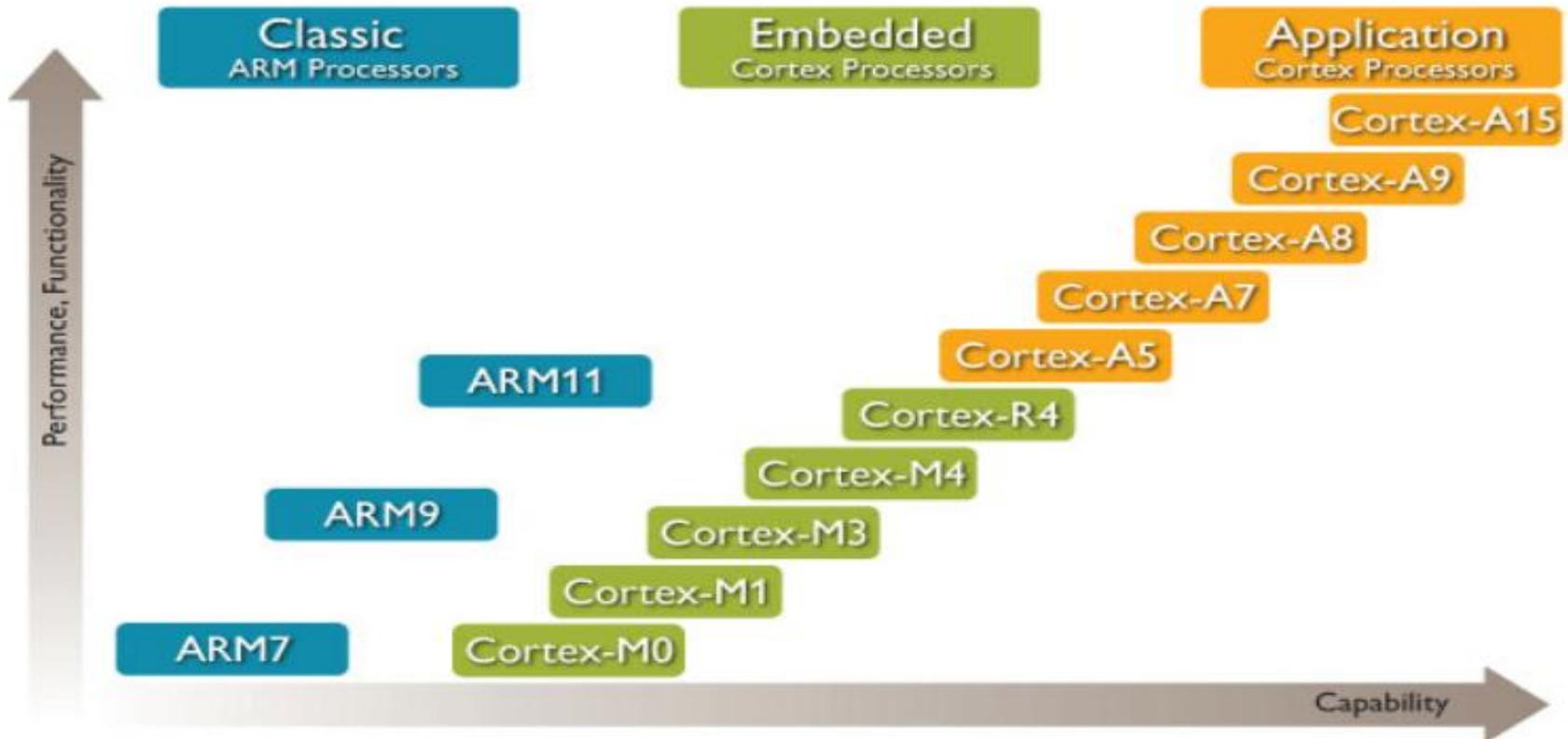
- Hierarchical processor integrating core and advanced system peripherals
- Cortex-M3 core
 - Harvard architecture
 - 3-stage pipeline w. branch speculation
 - Thumb[®]-2 and traditional Thumb
 - ALU w. H/W divide and single cycle multiply
- Cortex-M3 Processor
 - Cortex-M3 core
 - Configurable interrupt controller
 - Bus matrix
 - Advanced debug components
 - Optional MPU & ETM (Not available in STM32F10x)



Cortex-M3 Microprocessor



Processors for All Applications





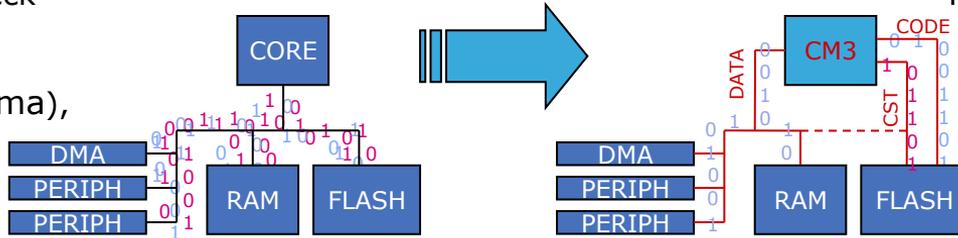
Bus system

Architecture of the bus

Cortex M3 Architecture: Harvard benefits with Von Neumann single memory space

Von Neumann "bottleneck"
Single 32bit bus for:

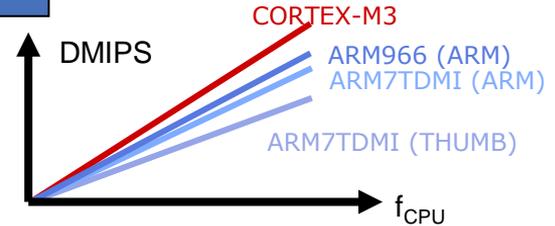
- code execution,
- data transfer (core/dma),
- peripheral control



Three 32bit buses for a parallel

- code execution,
- data transfer (core/dma),
- peripheral control

Outstanding efficiency of 1.25 DMIPS/MHz



THUMB2 instruction set provides 32bit performance with 16bit code density

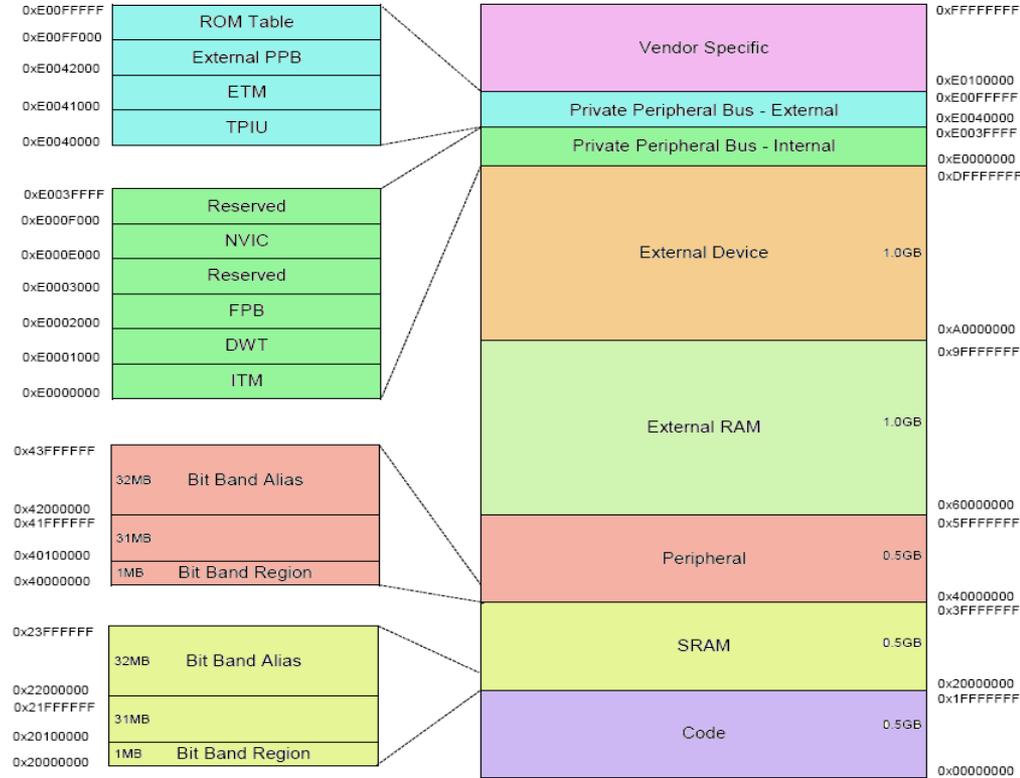
- THUMB 16bit Instruction Set → Full THUMB compatibility
- ARM 32bit Instruction Subset → Complete ARM instruction set for better performance
- New 16/32bit Instructions → 1 cycle MAC and Hardware Divide
Unaligned data, Bit banding

THUMB-2

- Single POWERFUL instruction set → No more mode switching
- 25% smaller code
- 25% lower RAM requirement

Cortex-M3 Memory Map

- **Vendor Specific (0.5GB)**
 - Set aside to enable vendors to implement peripheral compatibility with previous systems
- **Private Peripheral Bus (1M)**
 - Address space for system components (CoreSight, NVIC etc.)
- **External Device (1GB).**
 - Intended for external devices and/or shared memory that needs ordering/non-buffered
- **External RAM (1GB)**
 - Intended for off chip memory
- **Peripheral (0.5G)**
 - Intended for normal peripherals. The bottom 1MB of the 32MB peripheral address space (0x40000000 – 0x400FFFFFF) is reserved for bit-band accesses. Accesses to the peripheral 32MB bit band alias region (0x42000000 – 0x43FFFFFF) are remapped to this 1MB
- **SRAM (0.5GB)**
 - Intended for on-chip SRAM. The bottom 1MB of the SRAM address space (0x20000000 - 0x200FFFFFF) is reserved for bit-band accesses. Accesses to the SRAM 32MB bit band alias region (0x22000000 – 0x23FFFFFF) are remapped to this 1MB address space.
- **Code(0.5GB)**
 - Reserved for code memory (flash, SRAM). This region is accessed via the Cortex-M3 ICode and DCode busses.



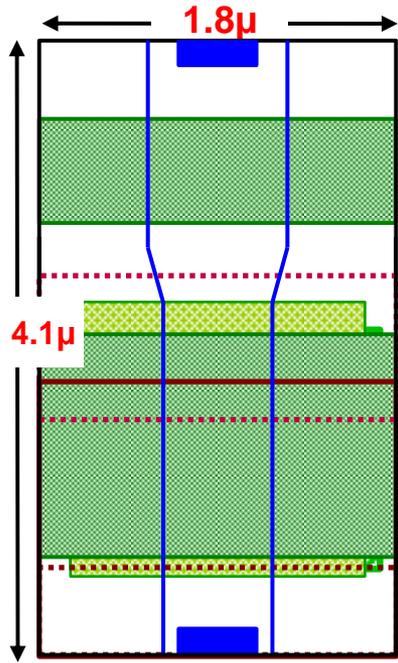


Production Technologies

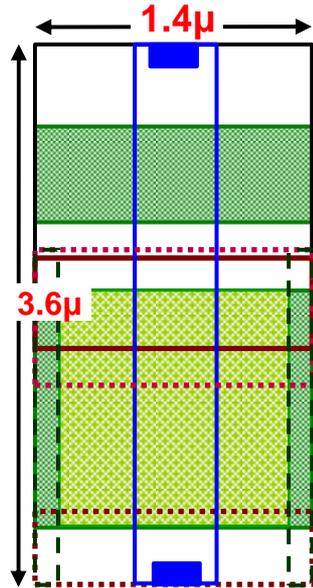
- The road to success...

CMOSF9 eEEPROM Technology History

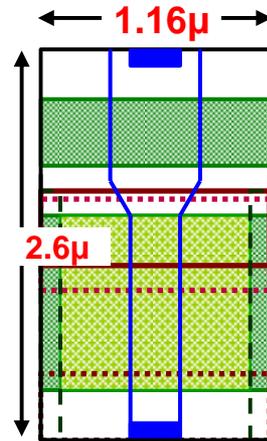
STMicroelectronics designs and manufactures embedded EEPROM products since 1988 for Microcontroller and Smartcard applications.



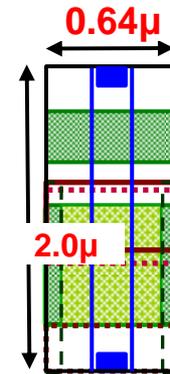
0.35µ
F6Y s=7.4µ²



0.18µ
F8 s=5.04µ²



0.15µ
F8N s=3.02µ²



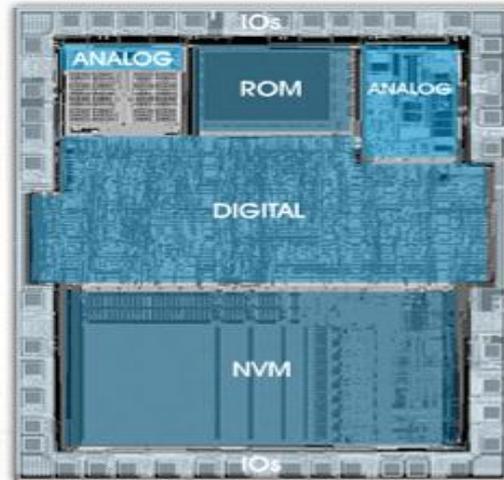
0.13µ
F9 1.28µ²

Beside embedded EEPROM each technology node contains also a sister technology with embedded flash. Today the 65nm node is being developed.

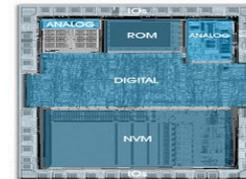
Technology to Break Price Barriers

- Technology driven development
- Breakthrough with 130nm lithography
- E² non-volatile memory, analog and digital peripherals

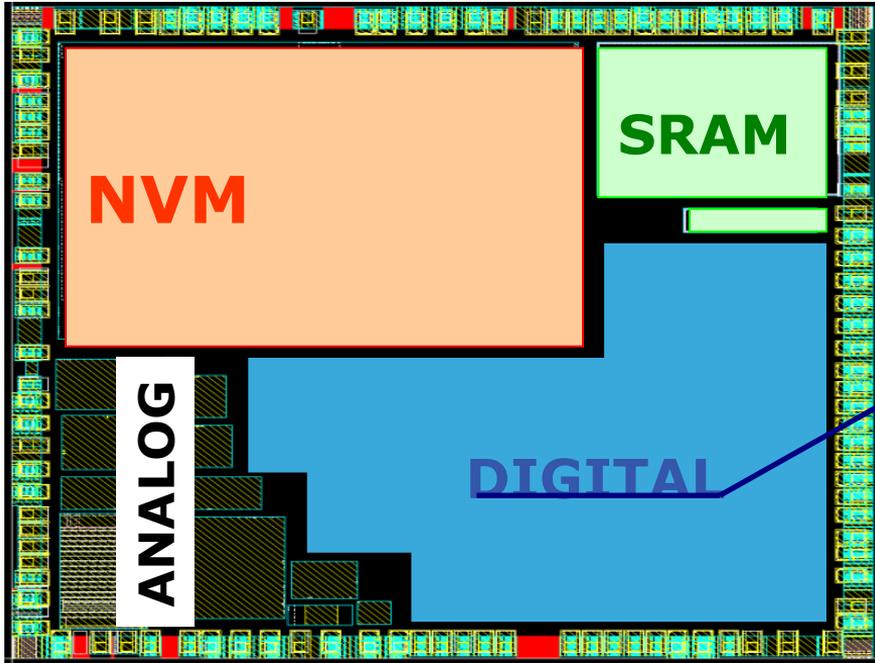
0,4μM



0,13μm



What part can be shrunk with production technologies?



Total digital bloc is **25% of the die size**

The CPU represents **30% of the digital area**

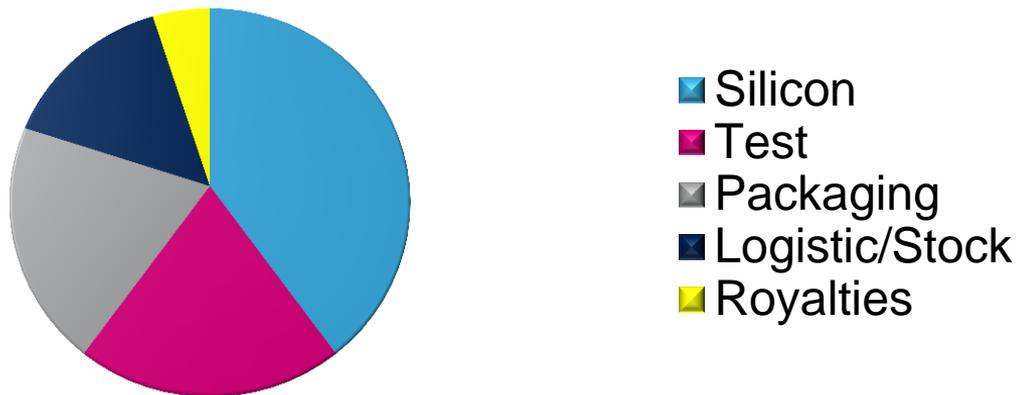
Cortex M0 is half gate count of M3 for the same configuration

Using M0 instead of M3 would lead to :

- **Less than 4% die area gain**
- **Less than 2% product cost gain**

Example of Cost Distribution for a MCU

Cost share



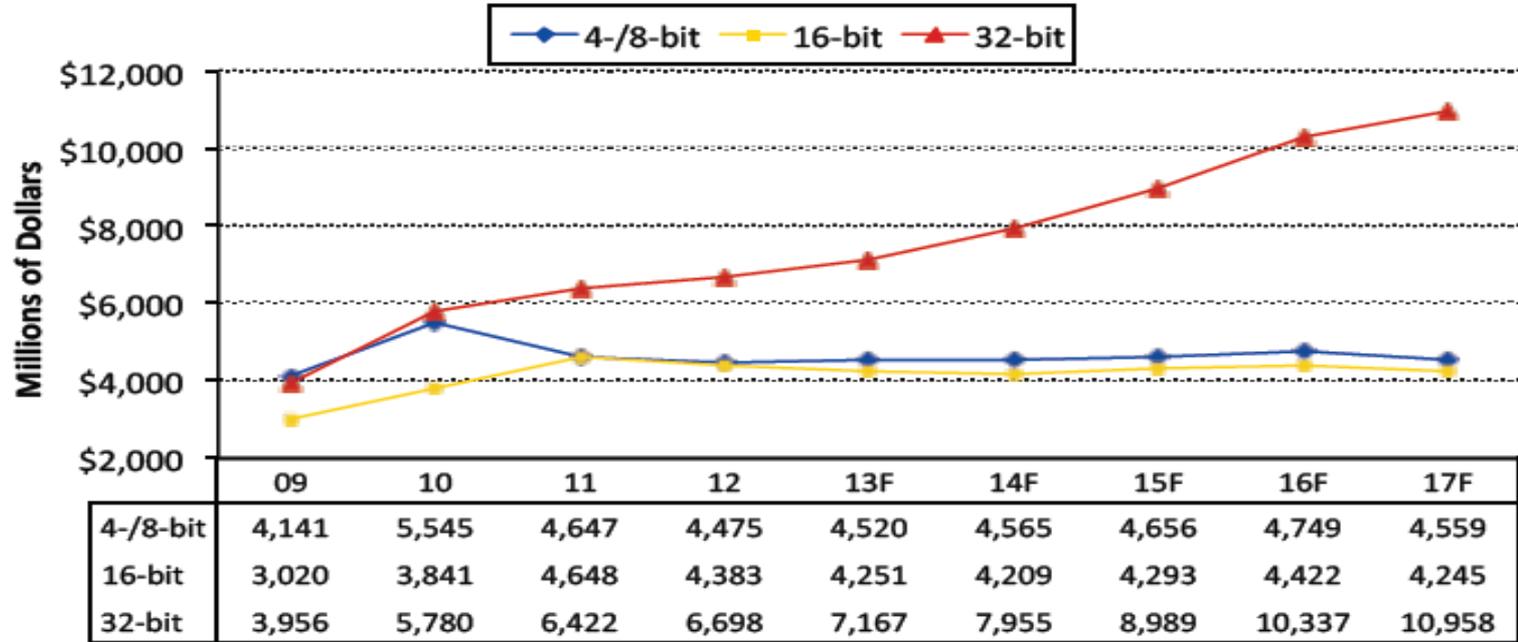
- Majority of the cost is not coming from the silicon itself
- The smaller the die size, the higher the non silicon cost
- Focusing all the innovation in the silicon is not the only way to decrease the cost



How do we think when we design a MCU?

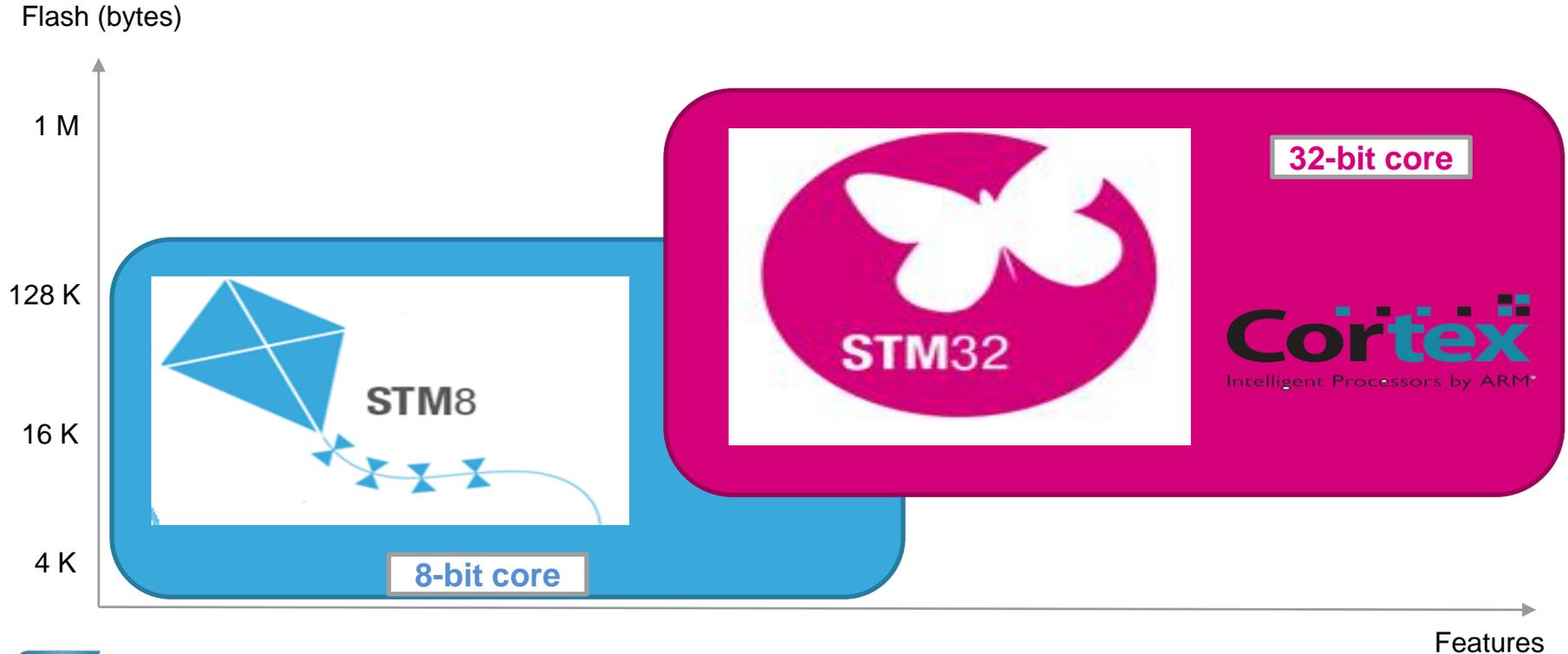
MCU market forecast

MCU Sales by Category (2009-2017)



Source: IC Insights

ST MCUs – strategy



Minimal External Components

- **Built-in Supervisor reduces need for external components**
 - Filtered reset input, Power-On reset, Low-Voltage Detect, Brown-Out Detect, Watchdog Timer with independent clock
- **One main crystal drives entire system (with help from PLL)**
 - Inexpensive 4-16 MHz crystal drives CPU, USB, all peripherals
- **Embedded 8 MHz RC can be used as main clock**
 - Optional 32 kHz crystal needed additionally for RTC, can run on internal 40 kHz RC
- **Only 7 external passive components for base system on LQFP100 package!!**

ST has licensed all Cortex-M processors

- Forget traditional 8/16/32-bit classifications and get
 - Seamless architecture across all applications
 - Every product optimized for ultra-low power and ease of use

Cortex-M0

8/16-bit applications

Cortex-M3

16/32-bit applications

Cortex-M4

32-bit/DSC applications

Binary and tool compatible



Cortex-M Powerful & scalable instruction set

Floating Point Unit

DSP (SIMD, fast MAC)

Advanced data processing
Bit field manipulations

General data processing
I/O control tasks

VABS	VADD	VCMP	VCMP	VCVT	VCVTR	VDIV	VLDM		
VLDR	VMLA	VMLS	VMOV	VMRS	VMSR	VHUL	VNEG		
VNMLA	VNMLS	VNMUL	VPOP	VPUSH	VSQRT	VSTM	VSTR		
VSUB	VFMA	VFHS	VFNMA	VFNMS				Cortex-M4 FPU	
PKH	QADD	QADD16	QADD8	QASX	QDADD	QDSUB	QSAX	SEL	SHADD16
QSUB	QSUB16	QSUB8	SADD16	SADD8	SASX	SMLABT	SMLATB	SMLABT	SMLATB
SHADD8	SHASX	SHSAX	SHSUB16	SHSUB8	SMLABB	SMLALD	SMLAWB	SMLALD	SMLAWB
SMLATT	SMLAD	SMLALBB	SMLALBT	SMLALTB	SMLALTT	SMLALD	SMLAWB	SMUAD	SMULBB
SMLAWT	SMLS	SMLS	SMMLA	SMMLS	SMMUL	SMULBT	SMULTT	SMULBT	SMULTT
ADC	ADD	ADR	AND	ASR	B	SMULTB	SMULWT	SMULTB	SMULWT
CLZ	BFC	BFI	BIC	CDP	CLREX	SMULWB	SMUSD	SMULWB	SMUSD
CBNZ	CBZ	CMN	CMP	DBG	EOR	SSAT16	SSAX	SSAT16	SSAX
LDmia	LDmDB	LDR	LDRB	LDRBT	LDRD	SSUB16	SSUB8	SSUB16	SSUB8
LDREX	LDREXB	LDREXH	LDRH	LDRHT	LDRSB	SXTAB	SXTAB16	SXTAB	SXTAB16
LDRSBT	LDRSHT	LDRSH	LDRT	MCR	LSL	SXTAH	SXTB16	SXTAH	SXTB16
LSR	MCRR	MLS	HLA	MOV	MOVT	UADD16	UADD8	UADD16	UADD8
MRC	MRRC	MUL	MVN	NOP	ORN	UASX	UHADD16	UASX	UHADD16
ORR	PLD	PLDW	PLI	POP	PUSH	UHADD8	UHASX	UHADD8	UHASX
RBIT	REV	REV16	REYSH	ROR	RRX	UHSAX	UHSUB16	UHSAX	UHSUB16
			RSS	SBC	SBEF	UHSUB8	UMAAL	UHSUB8	UMAAL
			SDIV	SEV	SMLAL	UQADD16	UQADD8	UQADD16	UQADD8
			SMULL	SSAT	STC	UQASX	UQSAX	UQASX	UQSAX
			STMIA	STMDB	STR	UQSUB16	UQSUB8	UQSUB16	UQSUB8
			STRB	STRBT	STRD	USAD8	USADA8	USAD8	USADA8
			STREX	STREXB	STREXH	USAT16	USAX	USAT16	USAX
			STRH	STRHT	STRT	USUB16	USUB8	USUB16	USUB8
			SUB	SXTB	SXTH	UXTAB	UXTAB16	UXTAB	UXTAB16
			TBB	TBH	TEQ	UXTAH	UXTB16	UXTAH	UXTB16
			TST	UBFX	UDIV				
			UMLAL	UMULL	USAT				
			UXTB	UXTH	WFE				
			WFI	YIELD	IT				



Low-Power Leadership from ARM

STM32 – 7 product series

Common core peripherals and architecture:

Communication peripherals: USART, SPI, I ² C
Multiple general-purpose timers
Integrated reset and brown-out warning
Multiple DMA
2x watchdogs Real-time clock
Integrated regulator PLL and clock circuit
External memory interface (FSMC)
Up to 3x 12-bit DAC
Up to 4x 12-bit ADC (Up to 5 MSPS)
Main oscillator and 32 kHz oscillator
Low-speed and high-speed internal RC oscillators
-40 to +85 °C and up to 105 °C operating temperature range
Low voltage 2.0 to 3.6 V or 1.65/1.7 to 3.6 V (depending on series)
Temperature sensor

+

STM32 F4 series - High performance with DSP (STM32F405/415/407/417/427/437)

168 MHz Cortex-M4 with DSP and FPU	Up to 256-Kbyte SRAM	Up to 2-Mbyte Flash	2x USB 2.0 OTG FS/HS	3-phase MC timer	2x CAN 2.0B	SDIO 2x I ² S audio Camera IF	Ethernet IEEE 1588	Crypto/ hash processor and RNG
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STM32 F3 series - Mixed-signal with DSP (STM32F302/303/313/372/373/383)

72 MHz Cortex-M4 with DSP and FPU	Up to 48-Kbyte SRAM & CCM-SRAM	Up to 256-Kbyte Flash	USB 2.0 FS	2x 3-phase MC timer (144 MHz)	CAN 2.0B	Up to 7x comparator	3x 16-bit ΣΔ ADC	4x PGA
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STM32 F2 series - High performance (STM32F205/215/207/217)

120 MHz Cortex-M3 CPU	Up to 128-Kbyte SRAM	Up to 1-Mbyte Flash	2x USB 2.0 OTG FS/HS	3-phase MC timer	2x CAN 2.0B	SDIO 2x I ² S audio Camera IF	Ethernet IEEE 1588	Crypto/ hash processor and RNG
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STM32 F1 series - Mainstream - 5 product lines (STM32F100/101/102/103 and 105/107)

Up to 72 MHz Cortex-M3 CPU	Up to 96-Kbyte SRAM	Up to 1-Mbyte Flash	USB 2.0 OTG FS	3-phase MC timer	Up to 2x CAN 2.0B	SDIO 2x I ² S audio	Ethernet IEEE 1588
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STM32 F0 series – Entry level (STM32F050/051)

48 MHz Cortex-M0 CPU	Up to 8-Kbyte SRAM	Up to 64-Kbyte Flash	3-phase MC timer	Comparator	CEC
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STM32 L1 series - Ultra-low-power (STM32L151/152/162)

32 MHz Cortex-M3 CPU	Up to 48-Kbyte SRAM	Up to 384-Kbyte Flash	USB FS device	Up to 12-Kbyte EEPROM	LCD 8x40 4x44	Comparator	BOR MSI VScal	AES 128-bit
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STM32 W series - Wireless (STM32W108)

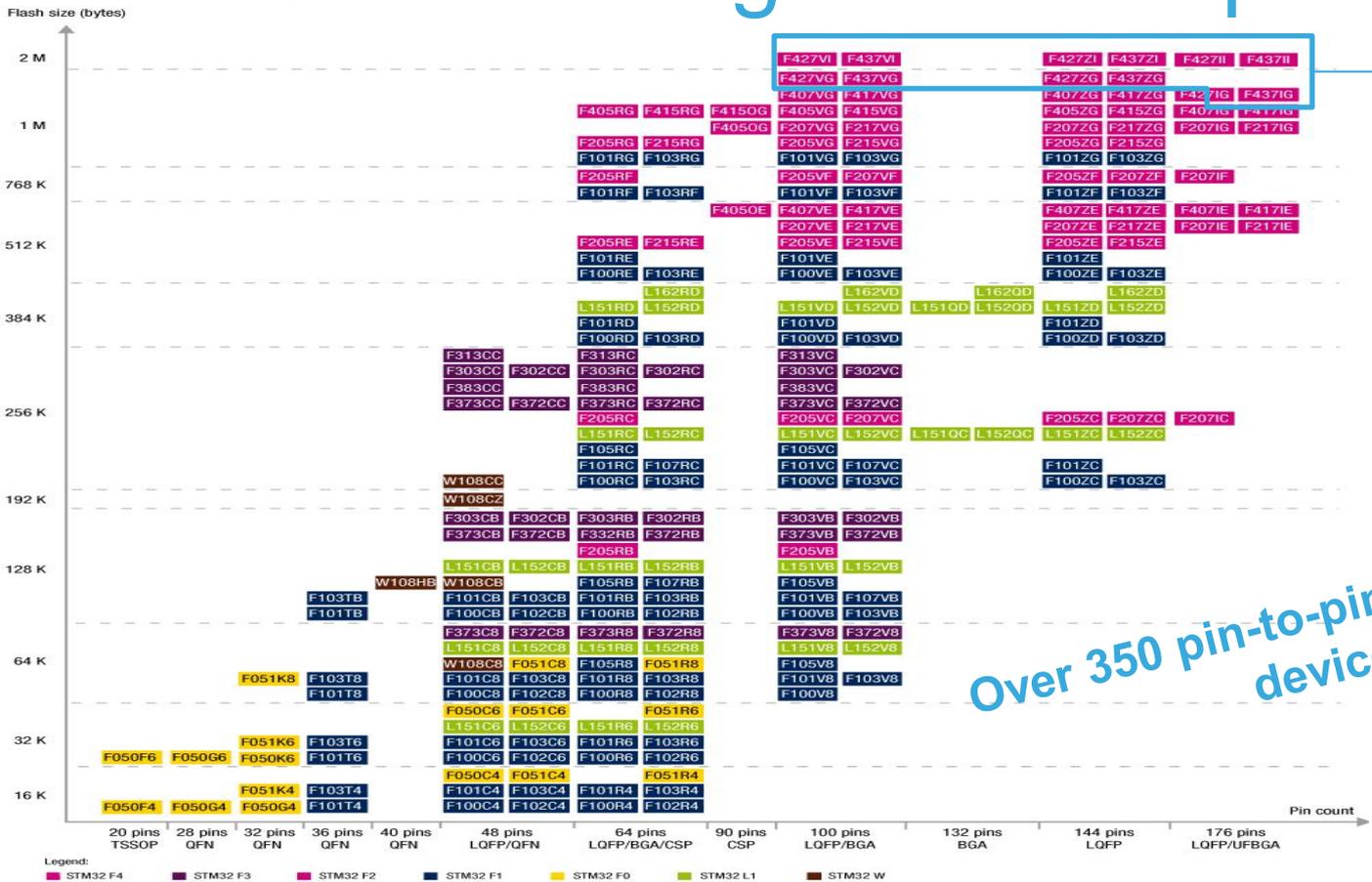
24 MHz Cortex-M3 CPU	Up to 16-Kbyte SRAM	Up to 256-Kbyte Flash	2.4 GHz IEEE 802.15.4 Transceiver	Lower MAC Digital baseband	AES 128-bit
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STM32 – leading Cortex-M portfolio



NEW 2 MB



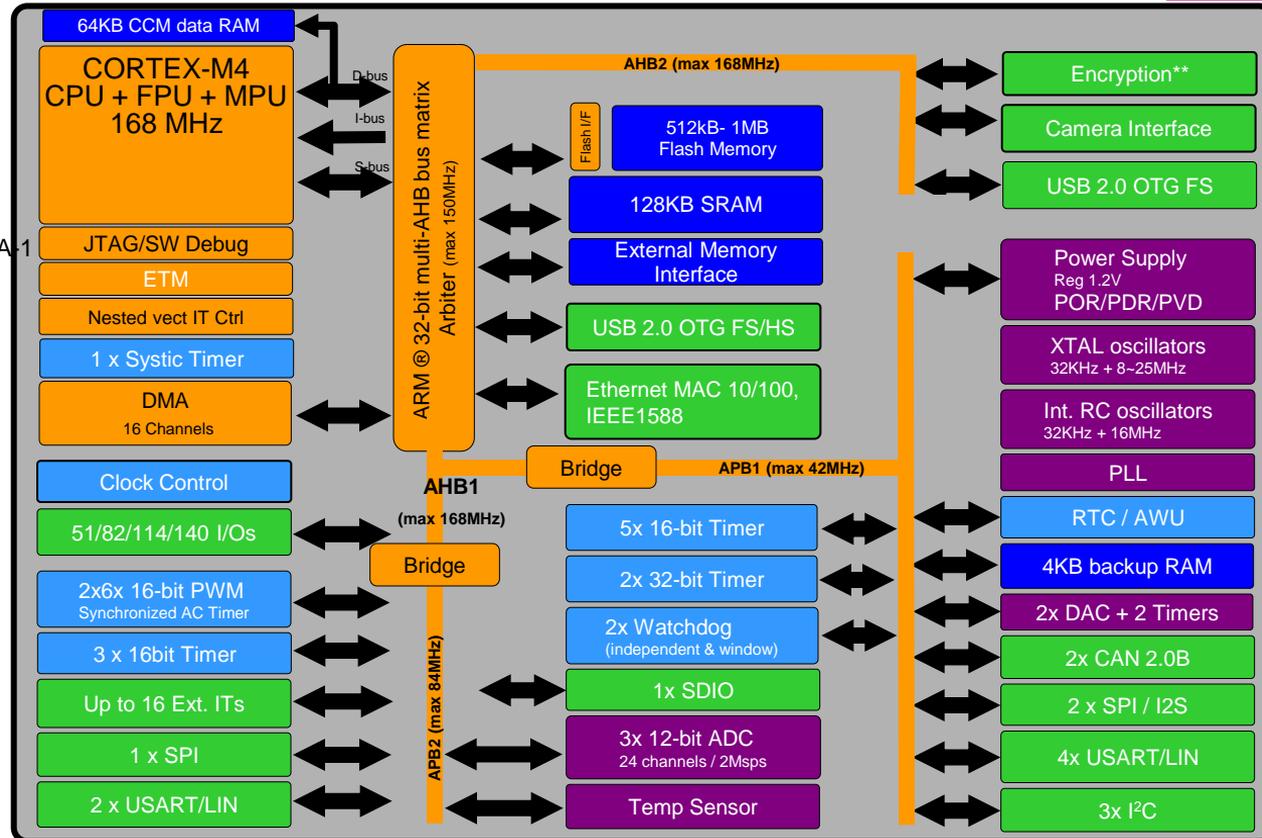
Over 350 pin-to-pin compatible devices



STM32F4xx Block Diagram

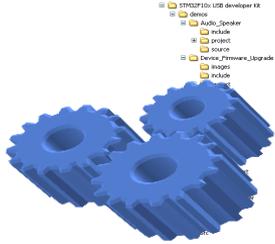
34

- Cortex-M4 w/ FPU, MPU and ETM
- Memory
 - Up to 1MB Flash memory
 - 192KB RAM including 64KB CCM data RAM
 - FSMC up to 60MHz
- New application specific peripherals
 - USB OTG HS w/ ULPI interface
 - Camera interface
 - HW Encryption**: DES, 3DES, AES 256-bit, SHA-1 hash, RNG.
- Enhanced peripherals
 - USB OTG Full speed
 - ADC: 0.416µs conversion/2.4MSPs, up to 7.2MSPs in interleaved triple mode
 - ADC/DAC working down to 1.8V
 - Dedicated PLL for I2S precision
 - Ethernet w/ HW IEEE1588 v2.0
 - 32-bit RTC with calendar
 - 4KB backup SRAM in VBAT domain
 - Pure 1% RC
 - 2 x 32bit and 8 x 16bit Timers
 - high speed USART up to 10.5Mb/s
 - high speed SPI up to 37.5Mb/s
- RDP (JTAG fuse)
- More I/O:s in UFBGA 176 package

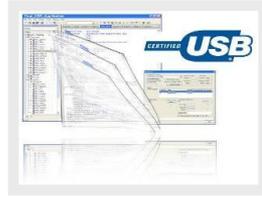


HS requires an external PHY connected to ULPI interface,
 ** Encryption is only available on STM32F415 and STM32F417

Free software solutions from ST



Standard Peripheral Library



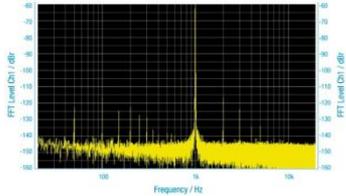
**USB device library
USB Host Library**



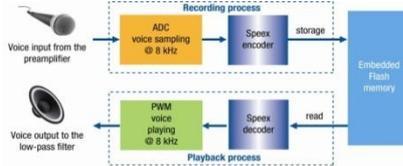
Motor Control Library



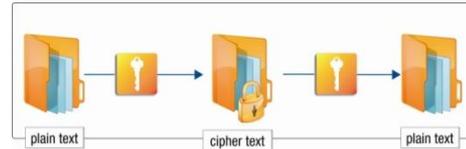
**Self-test routines for
EN/IEC 60335-1 Class B**



DSP Library



SPEEX Codec



Encryption Library

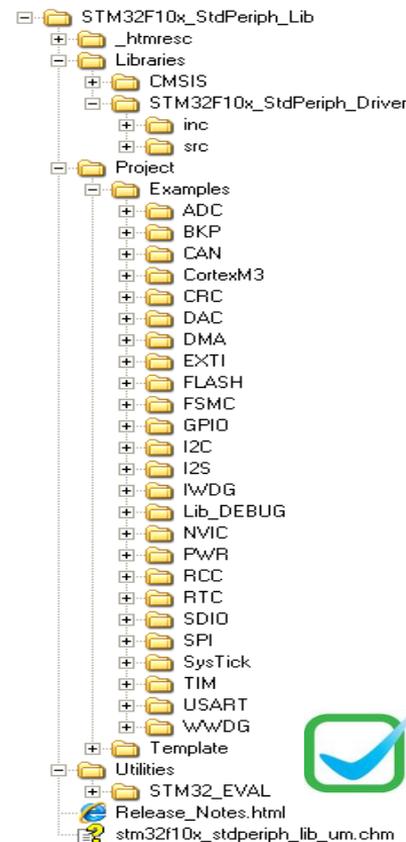


STM32 Audio Engine

Software libraries – speed time to market

36

- **ST software libraries free at www.st.com/mcu**
C source code for easy implementation of all STM32 peripherals in any application
 - **Standard library** – source code for implementation of all standard peripherals; code implemented in demos for STM32 evaluation board
 - **Motor control library** – sensorless vector control for 3-phase brushless motors
 - **USB Device Library** – Supporting HID, CDC, Audio, Mass Storage, DFU...)
 - **USB Host Library** – Supporting Mass Storage and HID
 - **DSP Library** – PID, IIR, FFT, FIR
 - **Graphics Library** – Drop down menus, radio buttons, sliders, ...
- **Software Solutions for**
 - Ethernet TCP/IP
 - Bluetooth
 - SpeexCodec
 - And many others.



- Evaluation board for full product feature evaluation

- **Hardware evaluation platform for all interfaces**
- **Connection to all I/Os and all peripherals**



STM32303C-EVAL
STM32373C-EVAL
Available in Q4-2012

(For any support before please contact our local ST office)

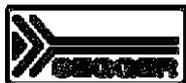
- Discovery kit for cost-effective evaluation and prototyping



STM32F3DISCOVERY
Available End Q3-2012

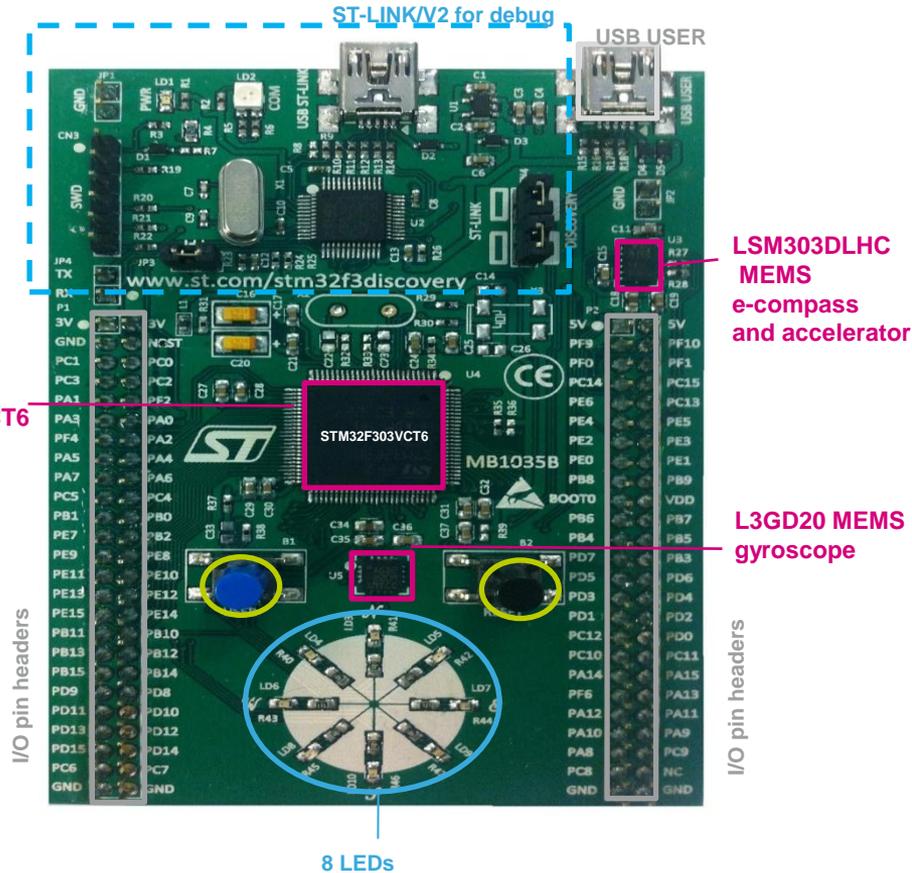
(For any support before please contact our local ST office)

- Large choice of IDE solutions from the STM32 and ARM ecosystem:



STM32F3-Discovery kit

- Includes everything for a quick start with the STM32F3 for less than \$11
- Ideal for evaluation, learning, prototyping
- The kit combines ST's STM32 F3 MCU with 9-axis MEMS sensors (gyroscope and e-compass), ready for 3D motion-sensing application development
- Dedicated web page: www.st.com/stm32f3discovery with SW example and documents

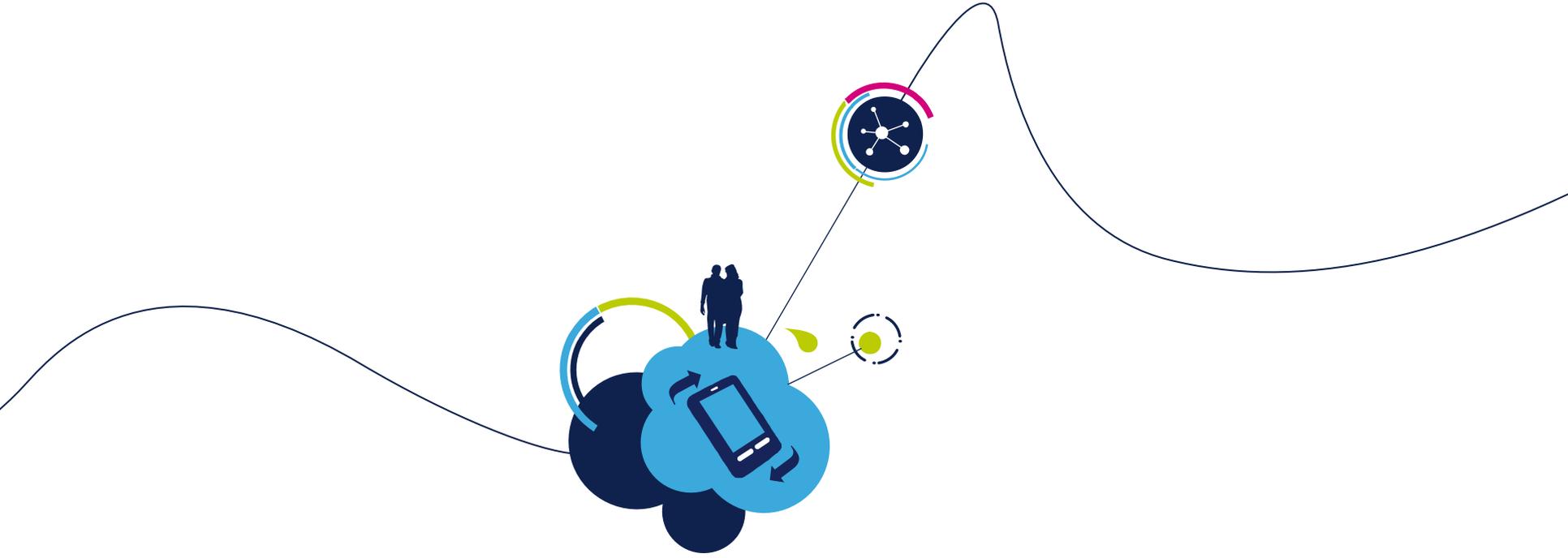




Future

MCU Trends – a selection of topics

- Price → Technology
- Performance → Low Power and MIPS
- Memory size → Larger flash and RAM
- Peripheral Integration → analog, RF
- Industry standard cores → Cortex Mx
- Advanced Peripherals → USB Ethernet LCD SDRAM
- Predefined Libraries + RTOS → Abstraction from the hardware



Q & A

After the session you should have learnt..

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- Differences between Harvard and Von Neuman Architecture
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Thank you

47

