Skriftlig Tentamen
IE1204 Digital Design
2022-10-28

Examiner/Examinator: Carl-Mikael Zetterling
Responsible teacher/Ansvarig lärare: Carl-Mikael Zetterling, 08-790 4344

Swedish/Svenska:
Tentamenstexten ska lämnas in när lösningarna lämnas in.
Inga tillåtna hjälpmedel utom linjal.
Examen består av två delar:
Del 1 har 16 uppgifter med max 1 poäng per uppgift som ska besvaras på "Answer Form".
Del 2 har 4 uppgifter med max 4 poäng per uppgift som ska besvaras på separat papper.
Lämna in båda delar samtidigt. Disponera tiden själv mellan delarna.
Uppgifterna är inte ordnade efter svårighetsgrad.
Om slutsumman av tentan har halvpoäng avrundas det uppåt.

X = 1 om studenten har minst 8 poäng på del 1
Y = 1 om studenten har minst 16 poäng totalt
P = 1 om studenter får godkänt på tentamen
Fx = 1 om studenten kan godkännas efter en extra uppgift

X	Y	P	Fx
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Totalt max 32 poäng på tentamen.
För godkänt krävs
(minst 8 poäng på del 1) OCH (minst 16 poäng totalt)
Fx om något villkor ej är uppfyllt med en poängs marginal.

Betygskalan för tentamen förutsatt att studenten har minst 8 poäng från del 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

Resultat meddelas inom tre veckor.

Written Exam
IE1204 Digital Design
2022-10-28

Examiner/Examinator: Carl-Mikael Zetterling
Responsible teacher/Ansvarig lärare: Carl-Mikael Zetterling, 08-790 4344

English:
The exam text should be handed in after the exam.
No aids allowed except ruler.
The exam consists of two parts:
Part 1 has 16 exercises for max 1 point per exercise to be answered on the "Answer Form".
Part 2 has 4 exercises for max 4 points per exercise, to be answered on a separate paper.
Hand in both parts at the same time. Plan the time yourself between the parts.
The exercises are not in order of difficulty.
If the total sum of the exam has half points this will be rounded up.

X = 1 if student has at least 8 points from part 1
Y = 1 if student has at least 16 points in total
P = 1 if student passes exam
Fx = 1 if a student can pass after an extra task

X	Y	P	Fx
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Total max of 32 points on the exam.
To pass the exam requires
(at least 8 points from part 1) AND (at least 16 points in total)
Fx if any condition is not fulfilled by one point's margin.

Grades are given as follows provided the student has at least 8 points from part 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

The result will be announced within three weeks.

Del 1/Part 1, 1 point per exercise, fill in on "Answer Form"

1 Number Conversion

Swedish: Konvertera de positiva talen och utför beräkningen.
Svara med ett decimalt tal.

English: Convert the unsigned numbers and perform the calculation.
Answer with a decimal number.

$Y = 100110_2 + 14_8 + 14_{10} + 14_{16}$
$= 38 + 12 + 14 + 20 = 84$

2 Addition

Swedish: Konvertera A och B från hexadecimala till 8 bitars två-komplement kodade tal.
Beräkna A + B (binärt) och svara med ett 8 bitars två-komplement kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: Convert A and B from hexadecimal to 8-bit binary (two's complement) numbers.
Calculate A + B (binary) and answer with an 8-bit binary (two's complement) number.
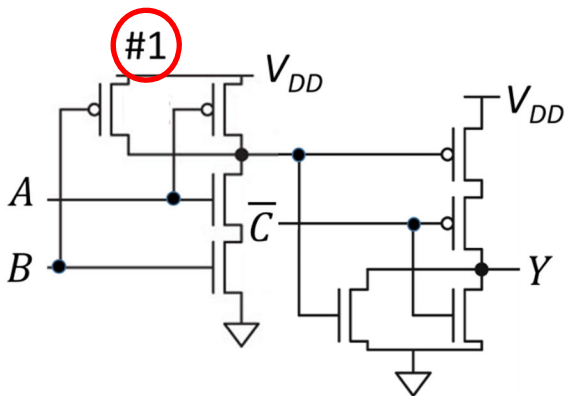You can check your calculations using decimal numbers.

$A = 0x62 = 62_{16}$ 01100010
$B = 0x1A = 1A_{16}$ $+ \underline{00011010}$
$A + B$ $= 01111100 = 0x7C$

3 Subtraction

Swedish: Konvertera A och B från hexadecimala till 8 bitars två-komplement kodade tal.
Beräkna A - B (binärt) och svara med ett 8 bitars två-komplement kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: Convert A and B from hexadecimal to 8-bit binary (two's complement) numbers.
Calculate A - B (binary) and answer with an 8-bit binary (two's complement) number.
You can check your calculations using decimal numbers.

$A = 0x35 = 35_{16}$ 00110101
$B = 0x78 = 78_{16}$ $= 01111000$
$- B =$ $+ \underline{10001000}$
$A - B$ $= 10111101 = 0xBD$

4 CMOS circuits

Swedish: Bestäm vilken/vilka av CMOS-grindnäten nedan som har den logiska funktionen Y.
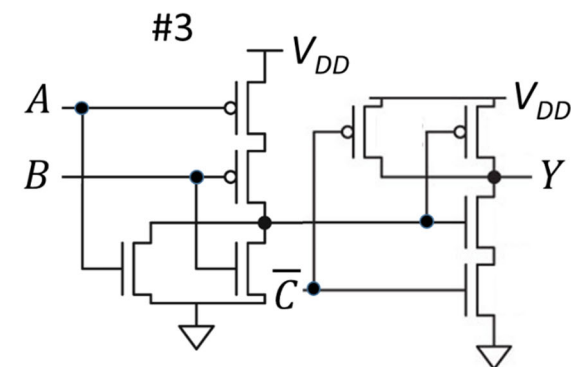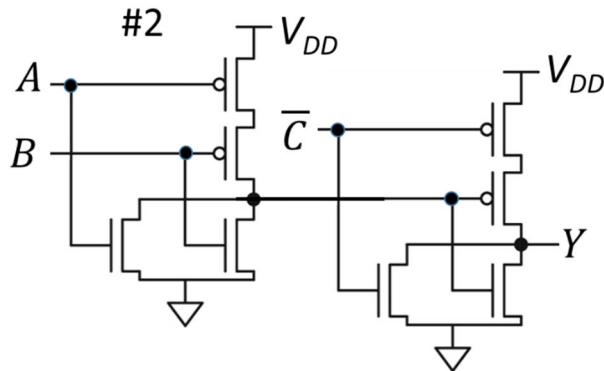Det kan finnas mer än ett korrekt svar.

English: Determine which of the CMOS-circuits below have the logic function Y.
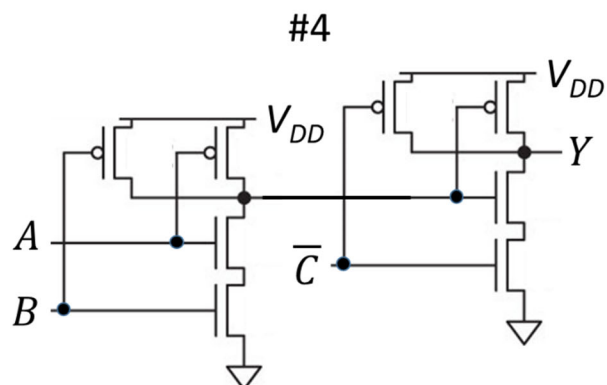There may be more than one correct answer.

$$Y = A \cdot B \cdot C$$

$$Y = \overline{\overline{A \cdot B} + \overline{C}} = \overline{\overline{A \cdot B \cdot C}} = A \cdot B \cdot C \qquad Y = \overline{\overline{A + B} + \overline{C}} = (A + B)C = A \cdot C + B \cdot C$$

$$Y = \overline{\overline{A + B \cdot C}} = \overline{\overline{A + B + C}} = A + B + C \qquad Y = \overline{\overline{A \cdot B} \cdot \overline{C}} = A \cdot B + C$$

5 Boolean Algebra

Swedish: Ta fram enklast möjliga booleska uttryck.

English: Derive the simplest possible Boolean expression.

$$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot C \cdot D + A \cdot B \cdot \overline{C} \cdot \overline{D} +$$
$$A \cdot B \cdot \overline{C} \cdot D + A \cdot B \cdot C \cdot D + A \cdot B \cdot C \cdot \overline{D} + A \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$$

$$\boxed{= B \cdot C \cdot D + \overline{C} \cdot \overline{D} + A \cdot B}$$
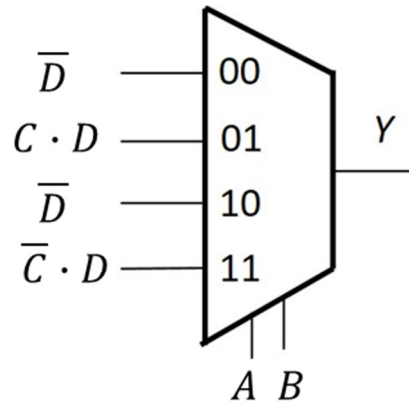
6 MUX to K-map

Swedish: Fyll i K-Map från MUX-kopplingen.
Ta fram enklast möjliga booleska uttryck för Y från K-map. Välj PoS eller SoP.

English: Fill in the K-Map from the MUX circuit.
Derive simplest possible Boolean expression from the K-map. Select PoS or SoP.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	0	0	1
AB 01	0	0	1	0
AB 11	0	1	0	0
AB 10	1	0	0	1

$$\overline{B} \cdot \overline{D} + \overline{A} \cdot B \cdot C \cdot D + A \cdot B \cdot \overline{C} \cdot D$$

7 K-Map to MUX

Swedish: Använd en 4:1 MUX och valfria grindar eller 0 och 1 och gör en krets för K-map med CD som select-signaler.

English: Use a 4:1 MUX and any logic gates or 0 or 1 to draw a circuit for the K-map with CD as select signals.
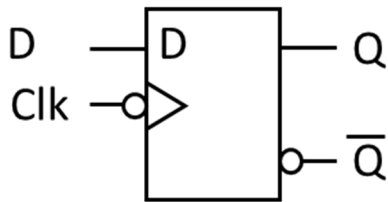
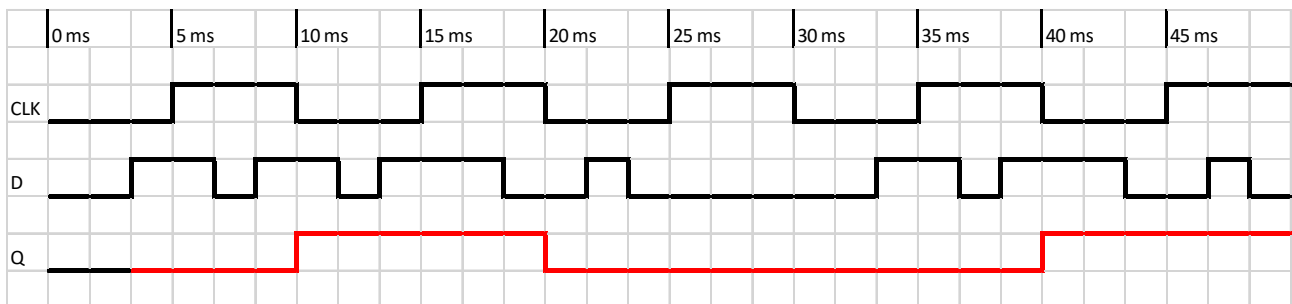| Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	0	1	0
AB 01	0	0	1	0
AB 11	1	0	0	1
AB 10	0	1	0	0
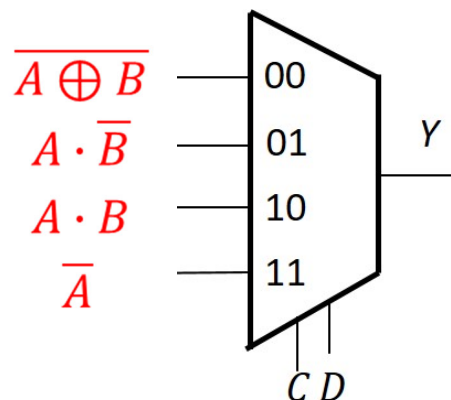
8 Timing diagram

Swedish: Rita tidsdiagram för D-vippan (D flip-flop) i "Answer Form".

English: Draw the timing diagram for the D flip-flop in the "Answer Form".

NOTE: negative edge

9 Timing diagram

Swedish: Rita tidsdiagram för JK-vippan (JK flip-flop) i "Answer Form".

English: Draw the timing diagram for the JK flip-flop in the "Answer Form".
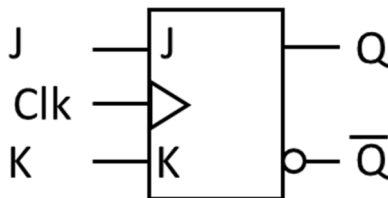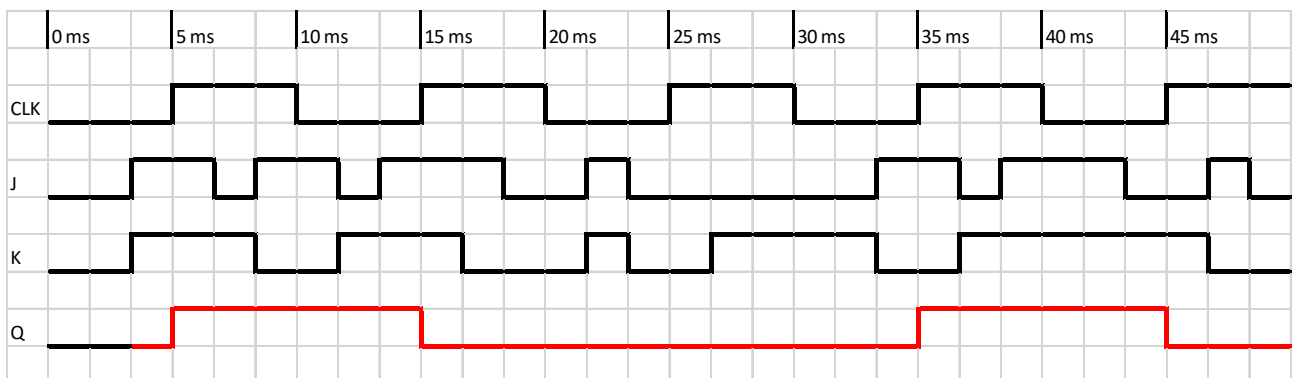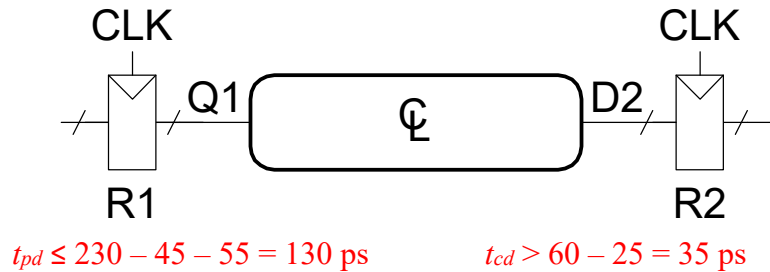

NOTE: positive edge

10 Timing calculation

Swedish: Beräkna fördröjningstiderna t_{pd} och t_{cd} för kretsen.

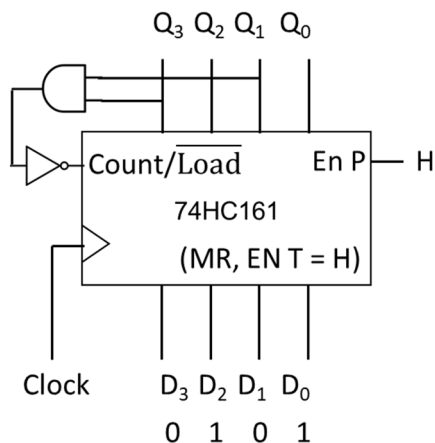**English:** Calculate the delay times t_{pd} and t_{cd} for the circuit.

t_{pcq} = 45 ps
t_{ccq} = 25 ps
t_{setup} = 55 ps
t_{hold} = 60 ps

T_c = 230 ps

$t_{pd} \leq 230 - 45 - 55 = 130$ ps $t_{cd} > 60 - 25 = 35$ ps

11 Counter analysis

Swedish: Räknaren nedan har kommit till tillstånd $Q_3Q_2Q_1Q_0 = 1010$.
Vad blir nästa tillstånd?

English: The counter below has counted to state $Q_3Q_2Q_1Q_0 = 1010$.
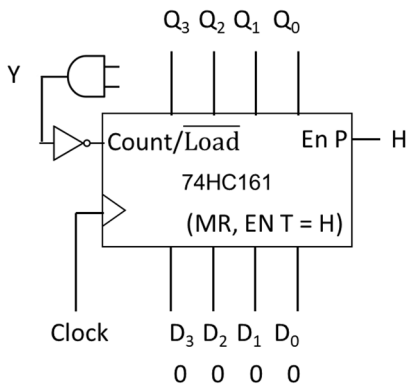What is the next state?

In the next state a load operation will be performed, and it is 0101 that is loaded

12 Counter design

Swedish: Hur ska AND-grinden kopplas för att få en räknare med 7 states? (dela med 7)

English: How should the AND-gate be connected to get a counter with 7 states? (divide-by-7)

The AND gate should detect 6, 0110, so
$Y = Q_2 \cdot Q_1$

13 Multiplication

Swedish: A och B är 8 bitars två-komplement kodade tal.
Beräkna A x B (binärt) och svara med ett 16 bitars två-komplement hexadecimalt kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.
Calculate A x B (binary) and answer with a 16-bit binary (two's complement) hexadecimal number.
You can check your calculations using decimal numbers.

$A = 00100110_2$
$B = 01111111_2$

A x B = B x A (both are positive) put B above since it has more '1's

```
        01111111
    x   00100110
      01111111   1st multiplication
    + 01111111    2nd multiplication
      1011111010
  + 01111111       3rd multiplication
    1001011011010 = 12DA₁₆
```

14 Division

Swedish: A och B är 8 bitars två-komplement kodade tal.
Beräkna A / B (binärt) och svara med kvot och rest
(8 bitars två-komplement hexadecimalt kodade tal).
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.
Calculate A / B (binary) and answer with quotient and remainder
(8-bit binary two's complement hexadecimal numbers).
You can check your calculations using decimal numbers.

$A = 01111111_2$
$B = 00101010_2$

A and B are both positive

```
              11   Quotient = 3
101010/01111111
      -  101010
         101011
      -  101010
              1   Remainder = 1
```

15 Full Adder

Swedish: Vad blir resultatet från heladderarkretsen nedan om switchen är satt på "0 (add)"?
Svara med 8 bitar (S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0). Ignorera carry out.
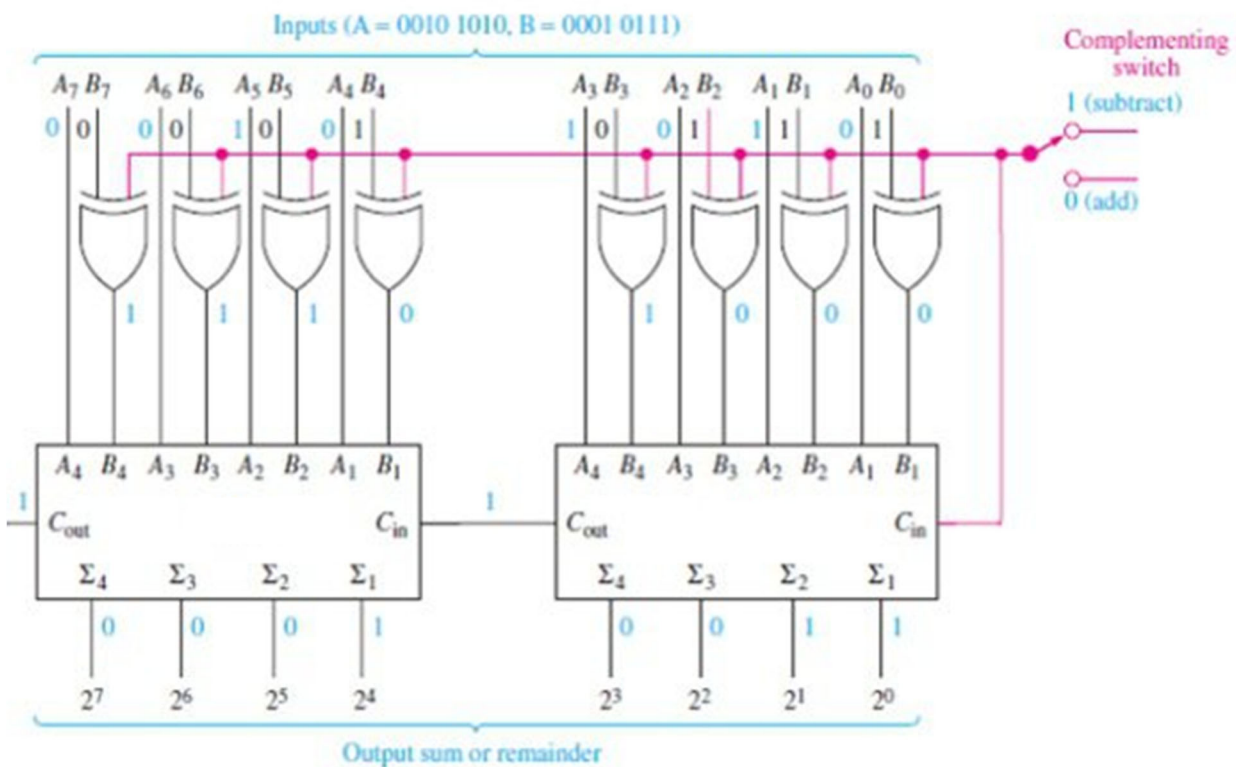
English: What is the result for the full adder circuit below if the switch is at "0 (add)"?
Answer with 8 bits (S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0). Ignore carry out.

Use these A and B (ignore the example in the figure).
A = 0011 0110
B = 0111 1000
    1010 1110

16 Shift register

Swedish: Ett skiftregistret har laddats med det binära talet Q.
Vad blir talet efter N klockpulser?
Svara med 8 bitar.

English: A shift register has been loaded with the binary number Q.
What is the result after N clock pulses?
Answer with 8 bits.

Operation = arithmetic shift right (ASR)
Q = 10011000_2 11100110 (sign bit is replicated in ASR)
N = 2

# Del 2/Part 2, 4 points per exercise, answer on separate paper

17 Analysis of Combinational Circuit

Swedish:
1. Ta fram booleskt uttryck för kretsen nedan.
2. Rita K-map för kretsen med variabelordning som i figuren.
3. Förenkla uttrycket med hjälp av K-map.
4. Rita ny krets med enbart NOR-grindar.

English:
1. Derive the Boolean expression for the circuit below.
2. Draw a K-map for the circuit with variables as in the figure.
3. Simplify the expression using the K-map.
4. Draw a new circuit using only NOR gates.
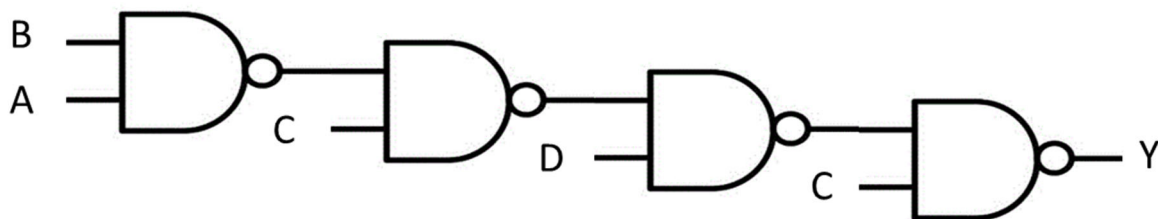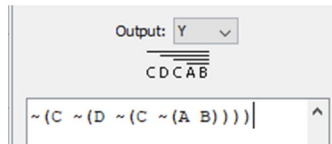

Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	1	0	0
AB 01	1	1	0	0
AB 11	1	1	1	0
AB 10	1	1	0	0

Rita om K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

Boolean expression and truth table

$$Y = \overline{\overline{C \cdot D} \cdot \overline{\overline{C} \cdot \overline{A} \cdot B}}$$

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

K-Map and simplified expressions
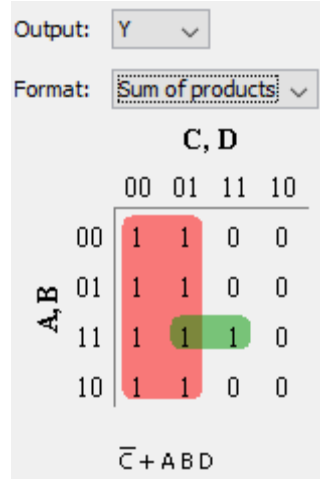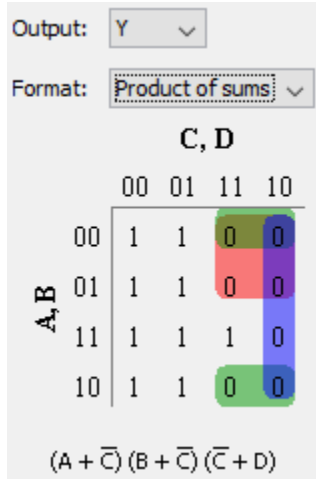
$(A + \overline{C})(B + \overline{C})(\overline{C} + D)$
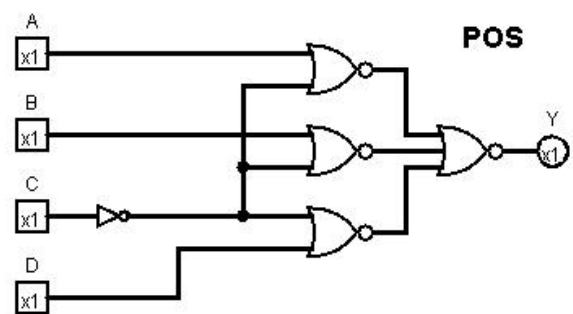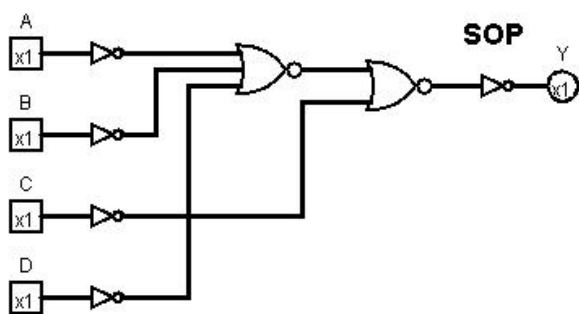
$\overline{C} + A\,B\,D$

Can be simplified with Boolean Algebra (not necessary for full points) or from SOP:

$$Y = \overline{\overline{C \cdot D} \cdot \overline{\overline{C} \cdot \overline{A} \cdot B}} = \overline{C} + D \cdot \overline{\overline{C} \cdot \overline{A} \cdot B} = \overline{C} + D \cdot \left(\overline{C} + \overline{\overline{A} \cdot B}\right) = \overline{C} + D \cdot \left(\overline{C} + A \cdot B\right)$$

$$= \overline{C} + D \cdot \overline{C} + A \cdot B \cdot D = \overline{C} + A \cdot B \cdot D = \overline{C} + \overline{\overline{A \cdot B \cdot D}} = \overline{C} + \overline{\overline{A} + \overline{B} + \overline{D}}$$

Or better from starting from POS since it is NOR (inverters can be made with NOR gates):

$$Y = (A + \overline{C})(B + \overline{C})(\overline{C} + D) = \overline{\overline{(A + \overline{C})(B + \overline{C})(\overline{C} + D)}} = \overline{\overline{A + \overline{C}} + \overline{B + \overline{C}} + \overline{\overline{C} + D}}$$

From original circuit using   Equivalence:
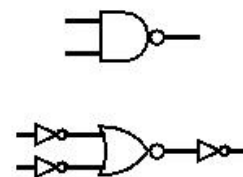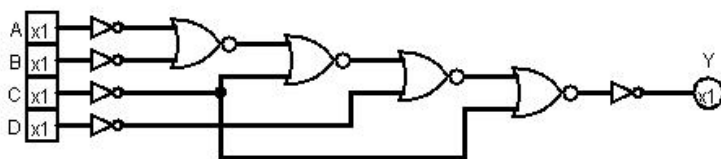
18 Design of Combinational Circuit

Swedish:

Konstruera kretsen för **e-segmentet** för en decimal 7-segmentsdekoder.
Sanningstabellen är given nedan.

1. Rita K-map för sanningstabellen med variabelordning som i figuren.
2. Uttnyttja x = don't care. Ta fram enklast möjliga booleska uttryck från K-map.
3. Rita en krets för uttrycket med enbart NAND-grindar.
4. Rita en krets för K-map som använder en 4:1 Mux, grindar och 0 och 1.

English:

Design the circuit for the **e-segment** of a decimal to 7-segment decoder.
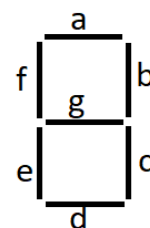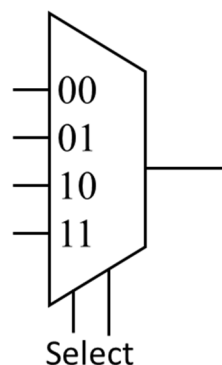The truth table is given below.

1. Draw a K-map for the truth table with variables as in the figure.
2. Use x = don't care. Derive simplest possible Boolean expression from the K-map.
3. Draw a circuit for the expression using only NAND-gates.
4. Draw a circuit for the K-Map using a 4:1 Mux, gates and 0 and 1.

e	CD 00	CD 01	CD 11	CD 10
AB 00	1	0	0	1
AB 01	0	0	0	1
AB 11	x	x	x	x
AB 10	1	0	x	x

Rita om K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

Inputs					Segments						
A	B	C	D		a	b	c	d	e	f	g
0	0	0	0		1	1	1	1	1	1	0
0	0	0	1		0	1	1	0	0	0	0
0	0	1	0		1	1	0	1	1	0	1
0	0	1	1		1	1	1	1	0	0	1
0	1	0	0		0	1	1	0	0	1	1
0	1	0	1		1	0	1	1	0	1	1
0	1	1	0		1	0	1	1	1	1	1
0	1	1	1		1	1	1	0	0	0	0
1	0	0	0		1	1	1	1	1	1	1
1	0	0	1		1	1	1	1	0	1	1
1	0	1	0		x	x	x	x	x	x	x
1	0	1	1		x	x	x	x	x	x	x
1	1	0	0		x	x	x	x	x	x	x
1	1	0	1		x	x	x	x	x	x	x
1	1	1	0		x	x	x	x	x	x	x
1	1	1	1		x	x	x	x	x	x	x

↑

K-Map and simplified expressions

Output: e ▼   Output: e ▼

Format: Sum of products ▼   Format: Product of sums ▼

C, D

	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	x	x	x	x
10	1	0	x	x

A, B

$$\overline{B}\,\overline{D} + C\,\overline{D}$$

C, D

	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	x	x	x	x
10	1	0	x	x

A, B

$$\overline{D}\,(\overline{B} + C)$$
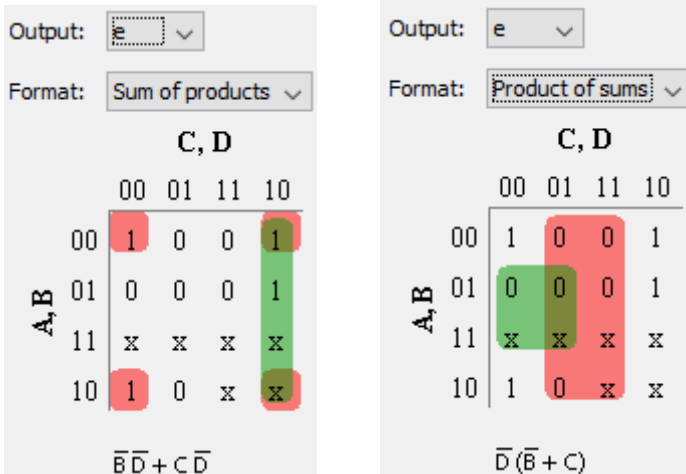
Use SOP for NAND only (inverters are ok if you note that they can be made with a NAND)
No deductions if not simplest possible.

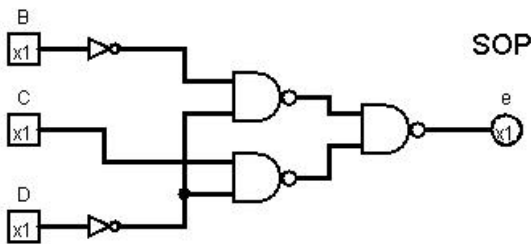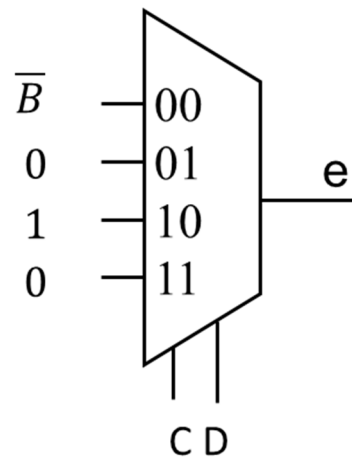$$Y_{SOP} = \overline{B} \cdot \overline{D} + C \cdot \overline{D} = \overline{\overline{\overline{B} \cdot \overline{D} + C \cdot \overline{D}}} = \overline{\overline{\overline{B} \cdot \overline{D}} \cdot \overline{C \cdot \overline{D}}}$$

$$Y_{POS} = \overline{D}(\overline{B} + C) = \overline{\overline{\overline{D} \cdot \overline{\overline{B} + C}}} = \overline{\overline{D} \cdot \overline{B \cdot \overline{C}}}$$

SOP

POS
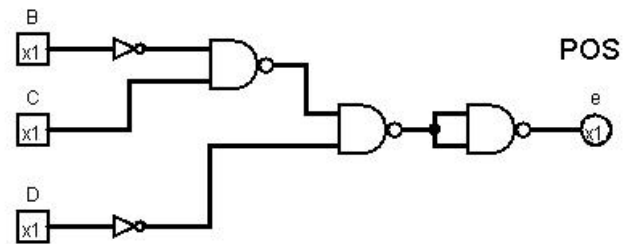
MUX (2 possibilities)
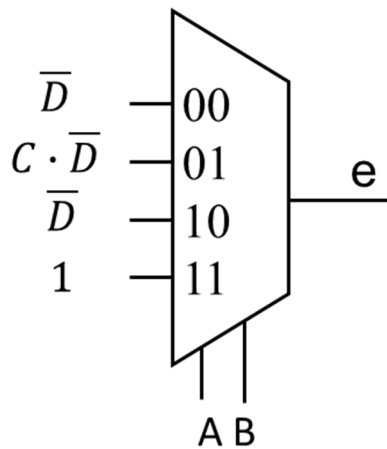
19 Analysis of FSM

Swedish: Analysera vad nedanstående tillståndsmaskin (FSM) utför.
1. Ta fram Boolska uttryck för nästa tillstånd Q3+ Q2+ Q1+ Q0+.
2. Rita K-Maps för Q3+ Q2+ Q1+ Q0+.
3. Rita tillståndstabell.
4. Rita tillståndsdiagram.

Använd ordningen Q3 Q2 Q1 Q0 (det finns inga utsignaler förutom tillståndsvariablerna)

English: Analyze the state machine (FSM) below.
1. Derive Boolean expressions for next state Q3+ Q2+ Q1+ Q0+.
2. Draw K-Maps for Q3+ Q2+ Q1+ Q0+.
3. Draw a state table.
4. Draw a state diagram.

Use the order Q3 Q2 Q1 Q0 (there are no outputs except for the state variables)
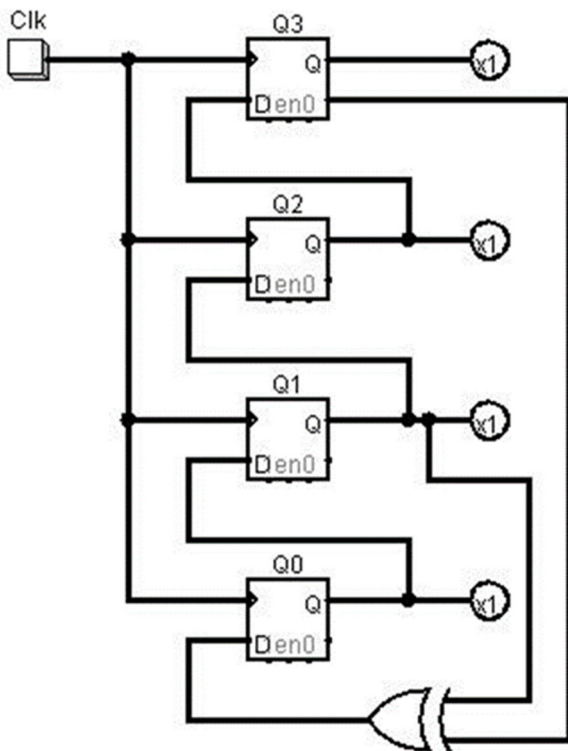
$Q_1Q_0 =$			
00	**01**	**11**	**10**

$Q_3Q_2 =$

00				
01				
11				
10				

> Rita om K-map i dina inlämnade svar.
>
> Redraw the K-map in your answer sheets.

$$Q_0^+ = \overline{Q_3} \oplus Q_1$$
$$Q_1^+ = Q_0$$
$$Q_2^+ = Q_1$$
$$Q_3^+ = Q_{02}$$

K-Maps and/or state table

Q3+ Q_3Q_2	Q_1Q_0 00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	0	0	0	0

Q2+ Q_3Q_2	Q_1Q_0 00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	0	1	1
10	0	0	1	1

Q1+ Q_3Q_2	Q_1Q_0 00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

Q0+ Q_3Q_2	Q_1Q_0 00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	1	1
10	0	0	1	1

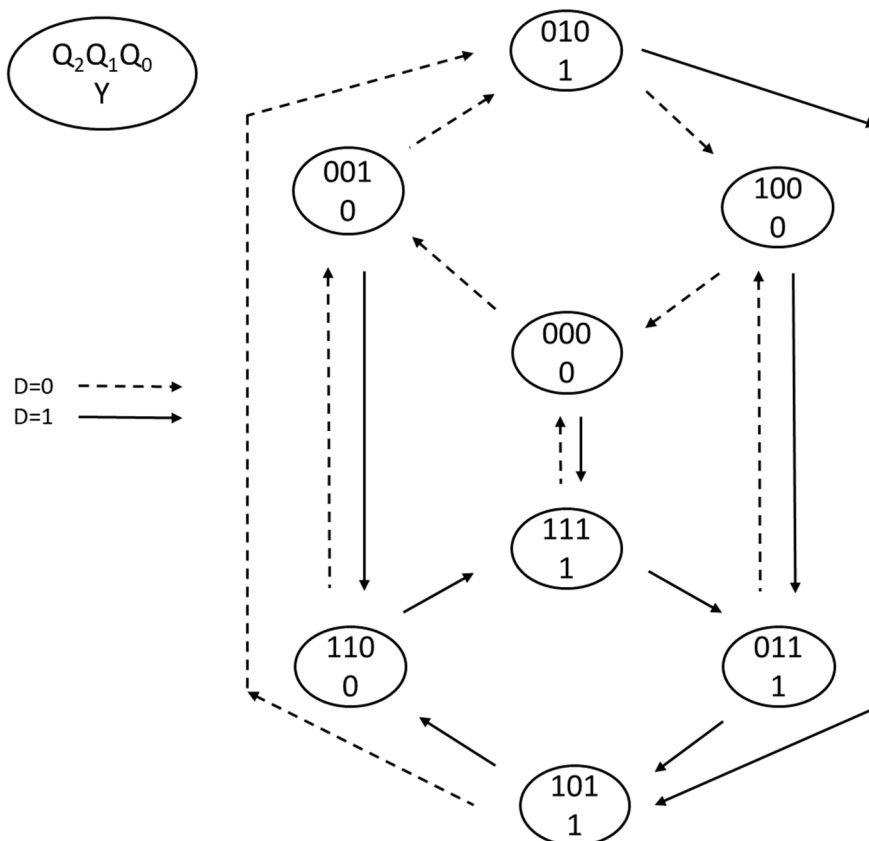| Present state				Next state			
Q3	Q2	Q1	Q0	Q3+	Q2+	Q1+	Q0+
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1
0	0	1	0	0	1	0	0
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	1
0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	0
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	1	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1

State diagram
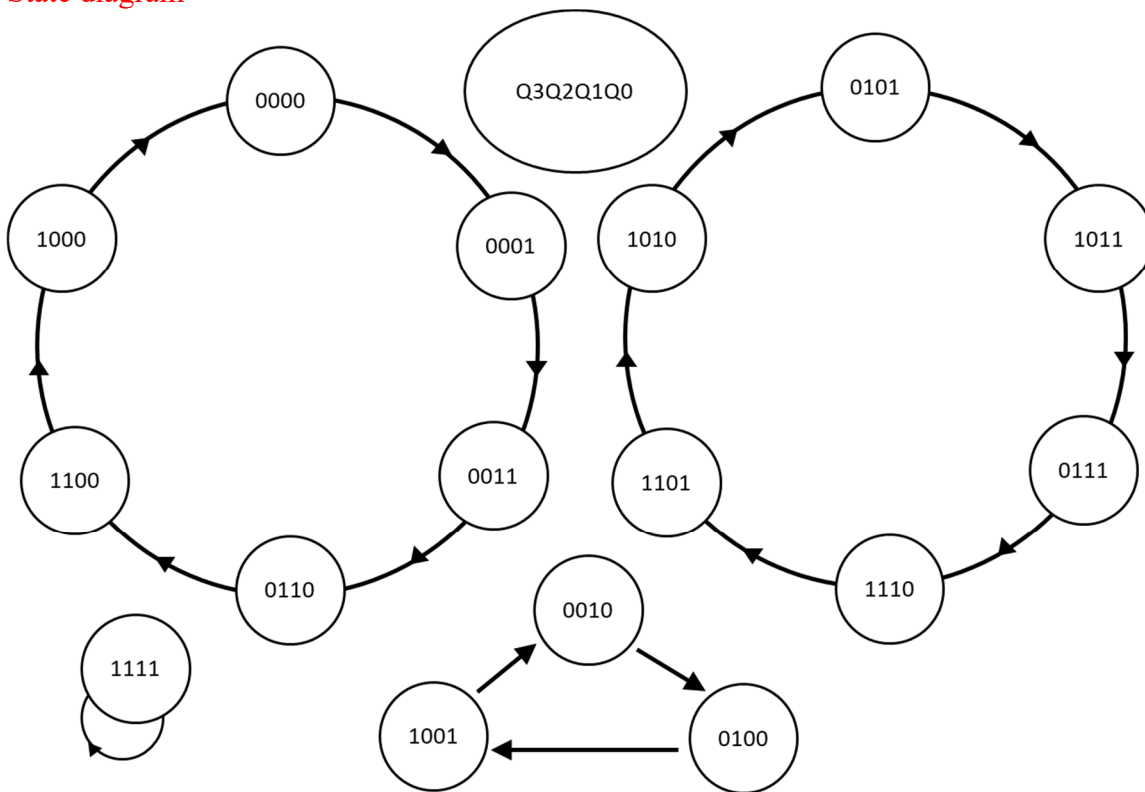
20 Design of FSM

Swedish: Konstruera en tillståndsmaskin (FSM) enligt tillståndsdiagrammet nedan.
1. Rita tillståndstabell.
2. Ta fram K-map för nästa tillstånd och utsignalen Y.
3. Ta fram minimerade uttryck för nästa tillstånd och utsignal. Använd "X" = don't care.
4. Rita kretsschema för en FSM med DFFs och vilka grindar som helst utom MUX.

English: Design a state machine (FSM) according to the state diagram below.
1. Draw a state table.
2. Derive K-maps for next state and output Y.
3. Derive minimized expressions for next state and output. Use "X" = don't care.
4. Draw the FSM circuit diagram with DFFs and any gates except MUX.

Rita om K-map i dina inlämnade svar.

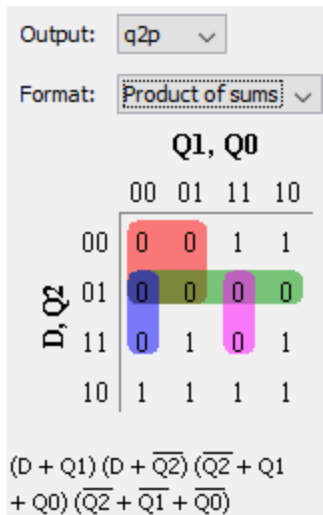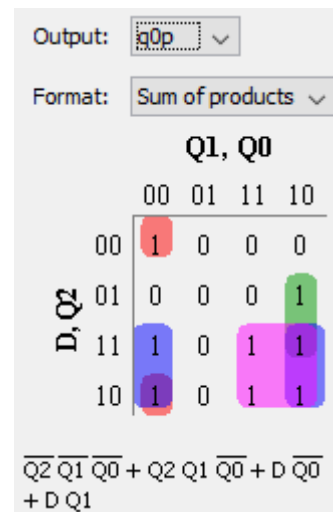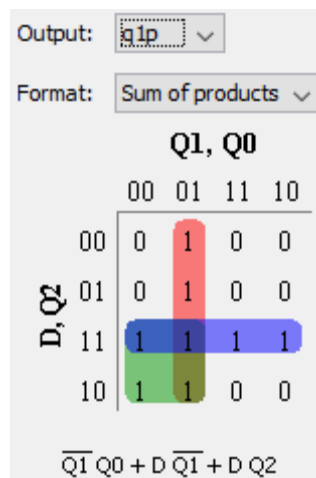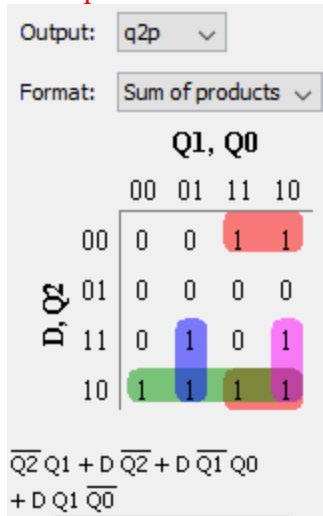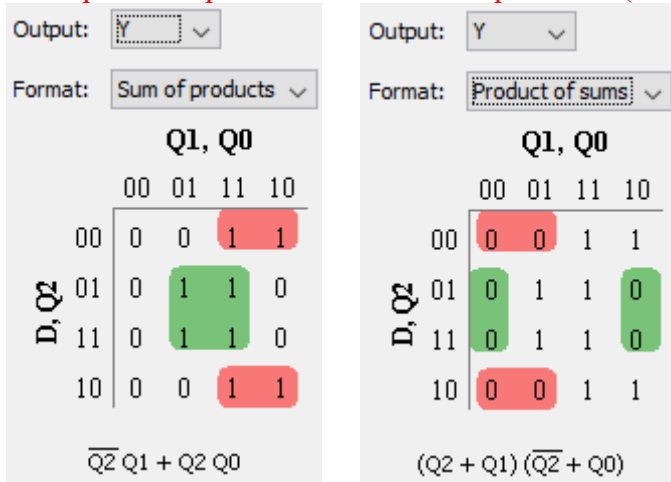Redraw the K-map in your answer sheets.

State table

Present state			Next state D = 0			Next state D = 1			Output
Q2	Q1	Q0	Q2+	Q1+	Q0+	Q2+	Q1+	Q0+	Y
0	0	0	0	0	1	1	1	1	0
0	0	1	0	1	0	1	1	0	0
0	1	0	1	0	0	1	0	1	1
0	1	1	1	0	0	1	0	1	1
1	0	0	0	0	0	0	1	1	0
1	0	1	0	1	0	1	1	0	1
1	1	0	0	0	1	1	1	1	0
1	1	1	0	0	0	0	1	1	1

K-Maps for next state with minimized expressions

Output: q2p
Format: Sum of products

$$\overline{Q2}\,Q1 + D\,\overline{Q2} + D\,\overline{Q1}\,Q0 + D\,Q1\,\overline{Q0}$$

Output: q1p
Format: Sum of products

$$\overline{Q1}\,Q0 + D\,\overline{Q1} + D\,Q2$$

Output: q0p
Format: Sum of products

$$\overline{Q2}\,\overline{Q1}\,\overline{Q0} + Q2\,Q1\,\overline{Q0} + D\,\overline{Q0} + D\,Q1$$

Output: q2p
Format: Product of sums

$$(D + Q1)(D + \overline{Q2})(\overline{Q2} + Q1 + Q0)(\overline{Q2} + \overline{Q1} + \overline{Q0})$$

Output: q1p
Format: Product of sums

$$(D + Q0)(D + \overline{Q1})(Q2 + \overline{Q1})$$

Output: q0p
Format: Product of sums

$$(D + \overline{Q0})(Q1 + \overline{Q0})(D + Q2 + \overline{Q1})(D + \overline{Q2} + Q1)$$

Output: Y
Format: Sum of products

Q1, Q0

	00	01	11	10
00	0	0	1	1
01	0	1	1	0
11	0	1	1	0
10	0	0	1	1

D, Q2

$\overline{Q2}\,Q1 + Q2\,Q0$

Output: Y
Format: Product of sums

Q1, Q0

	00	01	11	10
00	0	0	1	1
01	0	1	1	0
11	0	1	1	0
10	0	0	1	1

D, Q2

$(Q2 + Q1)\,(\overline{Q2} + Q0)$

FSM circuit diagram