

# IE1204 Digital Design Answer Form 2021-01-12

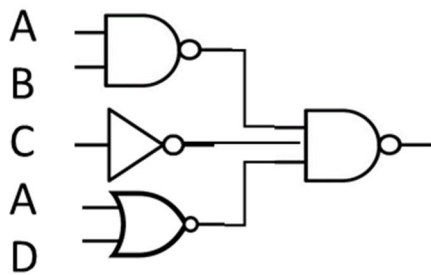
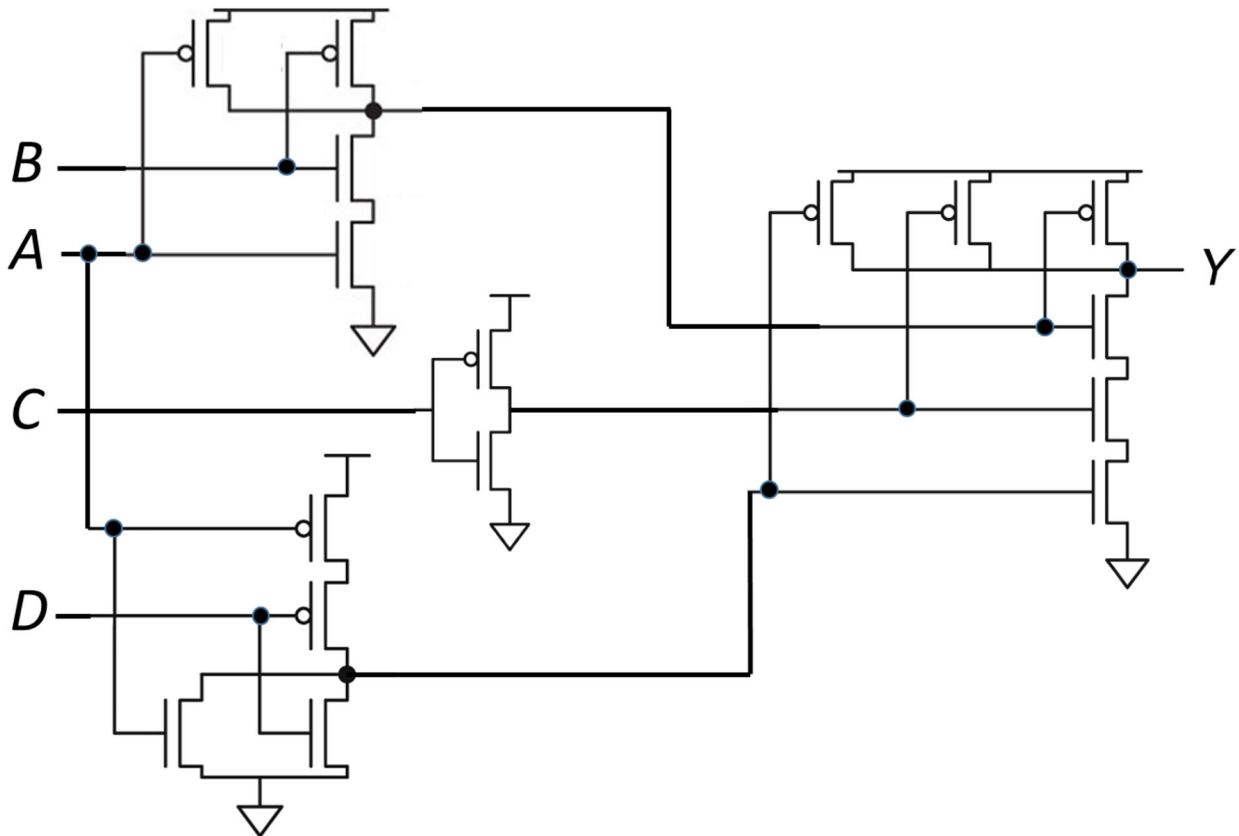
Full Name		Personal Number		Program						
Exam Answers 2021-01-12		YYYYMMDD-XXXX		NN						
#	Answer with	Answer				Points				
1	Decimal number	-42				1				
2	8 bit two's complement binary number	0	1	1	1	0	1	0	1	1
3	8 bit two's complement binary number	1	1	0	1	1	0	0	1	1
4	Boolean expression, Y =	$A + C + D$				1				
5	Boolean expression, Y =	$(A + B + \bar{C})(\bar{A} + \bar{B} + C)(\bar{A} + B + \bar{C})$				1				
6	Boolean expression, Y = OR	$(A + C)(\bar{B} + D)(\bar{A} + \bar{C})$ $\bar{A} \cdot \bar{B} \cdot C + \bar{A} \cdot C \cdot D + A \cdot \bar{B} \cdot \bar{C} + A \cdot \bar{C} \cdot D$				1				
7	MUX connections	$\overline{A \cdot B}$				1				
	Row CD = 00	$\bar{A}$								
	Row CD = 01	$\overline{A + B}$								
	Row CD = 10	$A \oplus B$								
	Row CD = 11									
8	Timing diagram					1				
9	Timing diagram					1				
10	Setup condition	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No		1					
	Hold condition	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No							
11	Boolean expression	$\bar{A} \cdot \bar{C}$				1				
12	16 bit two's complement binary number, MSB	1	1	1	1	1	1	1	0	1
	LSB	0	0	0	0	0	0	0	1	
13	8 bit two's complement binary number	1	1	1	0	1	1	0	1	1
14	Number interval	-64 to 63.5				1				
15	5 result bits (S4 S3 S2 S1 S0)	0 1 1 1 1				1				
16	4 flag bits (V C N Z)	0 0 1 0				1				
TOTAL POINTS		Examiner sign CMZ				16				

# IE1204 Digital Design Exam 2021-01-12 K-maps

## 4 CMOS

**Swedish:** Bestäm den logiska funktionen  $Y = f(A, B, C, D)$  för CMOS-grindnätet. Förenkla så långt som möjligt.

**English:** Determine the logic function  $Y = f(A, B, C, D)$  for the CMOS-circuit. Simplify as much as possible.



$$Y = \overline{\overline{(A \cdot B)} \cdot C} = A \cdot B + C + A + D = A + C + D$$

## 5 SoP / PoS

**Swedish:** Ta fram booleskt uttryck på PoS form för sanningstabellen nedan.

**English:** Derive the Boolean expression in PoS form for the truth table below.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

		AB			
		00	01	11	10
C	0	1	1	0	1
	1	0	1	1	0

$$Y = (A + B + \bar{C})(\bar{A} + \bar{B} + C)(\bar{A} + B + \bar{C})$$

## 6 K-map

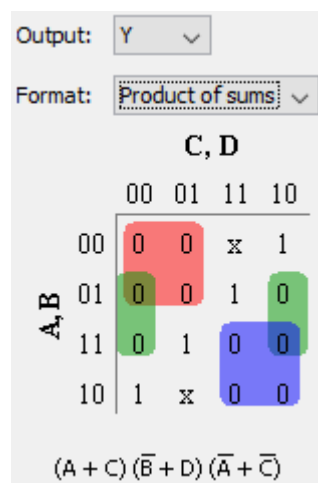
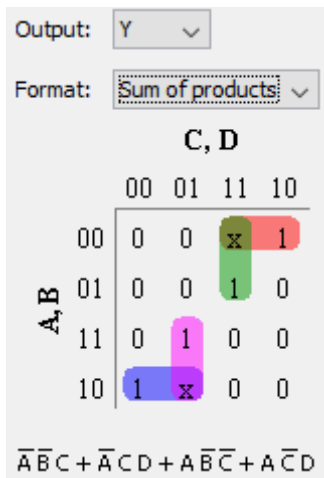
**Swedish:** Uttnyttja x = don't care.

Ta fram enklast möjliga booleska uttryck från K-map.

**English:** Use x = don't care.

Derive simplest possible Boolean expression from the K-map.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	0	0	X	1
AB 01	0	0	1	0
AB 11	0	1	0	0
AB 10	1	X	0	0



# IE1204 Digital Design Exam 2021-01-12 Solutions

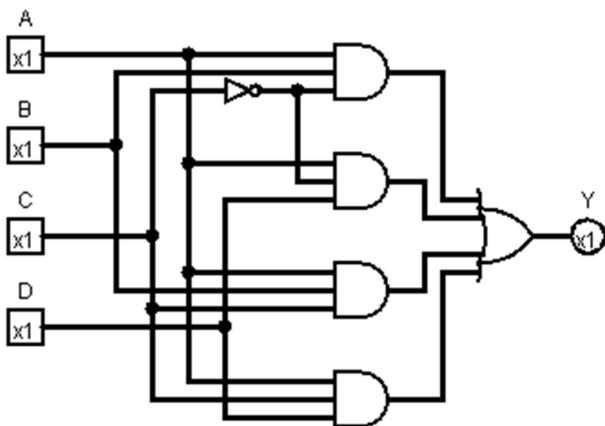
## 17 Analysis of Combinational Circuit

### Swedish:

1. Ta fram booleskt uttryck för kretsen nedan.
2. Rita K-map för kretsen med variabelordning som i figuren.
3. Förenkla uttrycket med hjälp av K-map.
4. Rita ny krets med enbart 2- och 3-ingångars NOR-grindar.

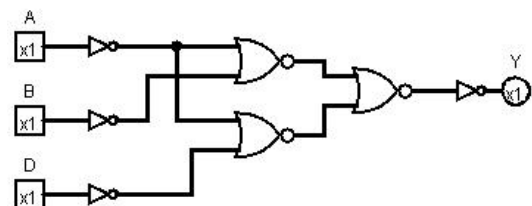
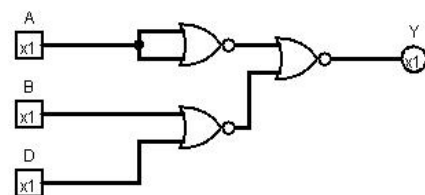
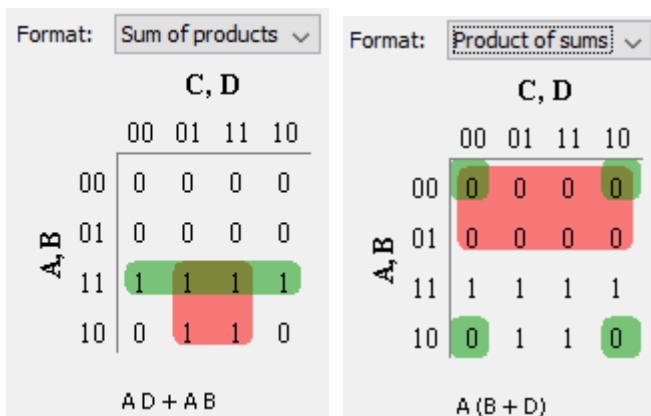
### English:

1. Derive the Boolean expression for the circuit below.
2. Draw a K-map for the circuit with variables as in the figure.
3. Simplify the expression using the K-map.
4. Draw a new circuit using only 2 and 3 input NOR gates.



Output:    
 $AB\bar{C} + A\bar{C}D + ABC + ACD$

**Use POS for NOR only (inverters are ok if you note that they can be made with a NOR)  
 No deductions if not simplest possible.**



For POS, draw  $Y = \overline{\overline{A + B + D}}$  (See top figure)

For SOP, draw  $Y = \overline{\overline{\overline{A} + \overline{D} + \overline{A} + \overline{B}}}$

(Note the double inversion bars, an extra inverter/NOR is needed)

## 18 Design of Combinational Circuit

### Swedish:

Designa en kombinatorisk krets för  $Y=f(Q_3, Q_2, Q_1, Q_0)$ ,  $Q_3 = \text{MSB}$  där

$Y = 1$  för alla tal som är jämt delbara med 3

$Y = x$  (don't care) för 7, 11, 13 och 14

$Y = 0$  för alla övriga tal

1. Rita sanningstabellen.
2. Rita K-map för sanningstabellen med variabelordning som i figuren.
3. Utnyttja  $x = \text{don't care}$ . Ta fram enklast möjliga booleska uttryck från K-map.
4. Rita en krets för uttrycket med enbart NAND-grindar.

### English:

Design a combinational circuit for  $Y=f(Q_3, Q_2, Q_1, Q_0)$ ,  $Q_3 = \text{MSB}$  where

$Y = 1$  for all numbers evenly divisible by 3

$Y = x$  (don't care) for 7, 11, 13, and 14

$Y = 0$  for all other numbers

1. Draw the truth table.
2. Draw a K-map for the truth table with variables as in the figure..
3. Use  $x = \text{don't care}$ . Derive simplest possible Boolean expression from the K-map.
4. Draw a circuit for the expression using only NAND-gates.

	$Q_1Q_0 =$			
	00	01	11	10
$Q_3Q_2 =$				
00				
01				
11				
10				

Rita om K-map i dina  
inlämnade svar.

Redraw the K-map in  
your answer sheets.

(Answer on next page)

# 18 Design of Combinational Circuit

Version A: Zero not divisible by 3

Q3	Q2	Q1	Q0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	x
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	x
1	1	0	0	1
1	1	0	1	x
1	1	1	0	x
1	1	1	1	1

Format:

Q1, Q0

	00	01	11	10
Q3, Q2	0	0	1	0
0	0	0	x	1
1	1	x	1	x
0	0	1	x	0

Q1 Q0 + Q2 Q1 + Q3 Q0 + Q3 Q2

Format:

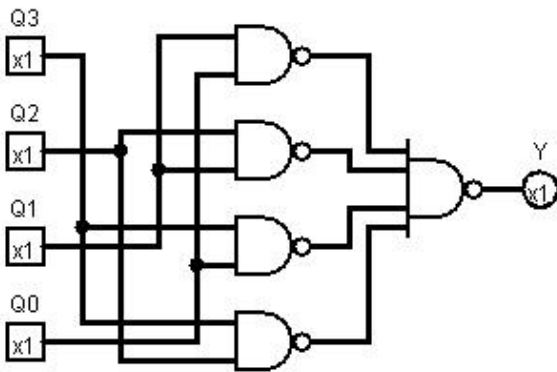
Q1, Q0

	00	01	11	10
Q3, Q2	0	0	1	0
0	0	0	x	1
1	1	x	1	x
0	1	x	0	0

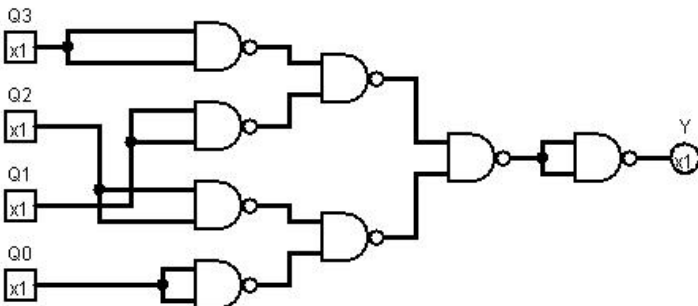
(Q3 + Q1) (Q2 + Q0)

**Use SOP for NAND only (inverters are ok if you note that they can be made with a NAND)  
No deductions if not simplest possible.**

For SOP draw  $Y = \overline{Q1 \cdot Q0 \cdot Q2 \cdot Q1 \cdot Q3 \cdot Q0 \cdot Q3 \cdot Q2}$  (see figure)



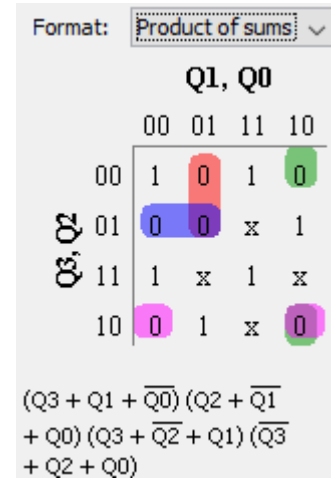
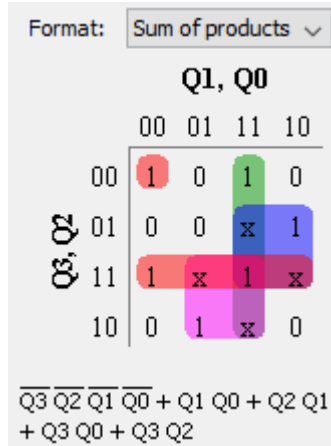
For POS draw  $Y = \overline{\overline{Q3} \cdot \overline{Q1} \cdot \overline{Q2} \cdot \overline{Q0}}$



(Note the double inversion bars, an extra inverter/NAND is needed)

Version B: Zero divisible by 3

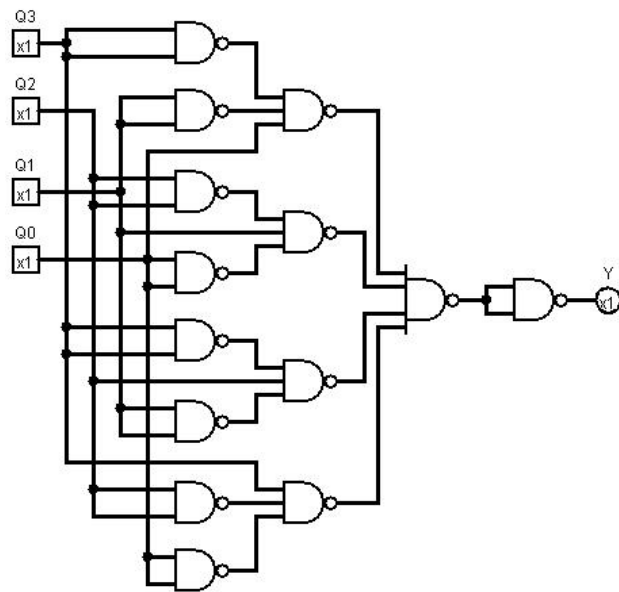
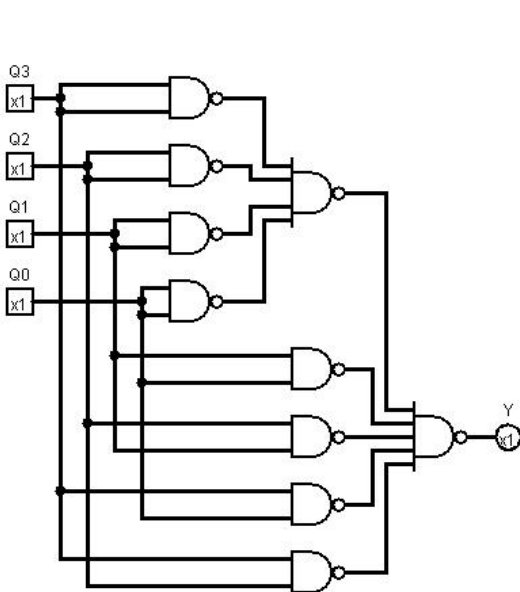
Q3	Q2	Q1	Q0	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	x
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	x
1	1	0	0	1
1	1	0	1	x
1	1	1	0	x
1	1	1	1	1



**Use SOP for NAND only (inverters are ok if you note that they can be made with a NAND)  
No deductions if not simplest possible.**

For SOP draw  $Y = \overline{\overline{\overline{Q3} \cdot \overline{Q2} \cdot \overline{Q1} \cdot \overline{Q0} \cdot \overline{Q1} \cdot \overline{Q0} \cdot \overline{Q2} \cdot \overline{Q1} \cdot \overline{Q3} \cdot \overline{Q0} \cdot \overline{Q3} \cdot \overline{Q2}}}}$  (see left figure)

For POS draw  $Y = \overline{\overline{\overline{\overline{Q3} \cdot \overline{Q1} \cdot \overline{Q0} \cdot \overline{Q2} \cdot \overline{Q1} \cdot \overline{Q0} \cdot \overline{Q3} \cdot \overline{Q2} \cdot \overline{Q1} \cdot \overline{Q3} \cdot \overline{Q2} \cdot \overline{Q0}}}}}}$  (see right figure)  
(Note the double inversion bars, an extra inverter/NAND is needed)





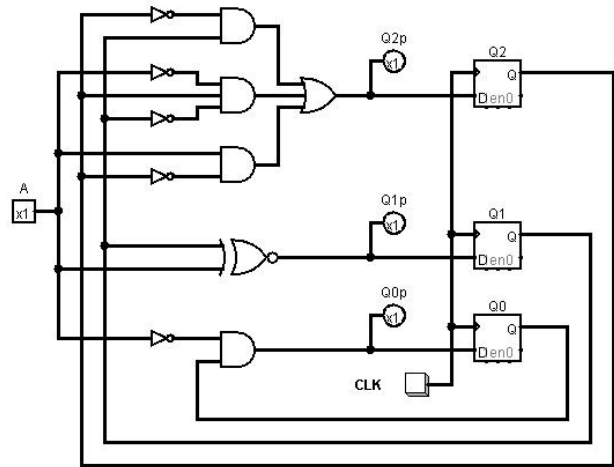
## 19 Analysis of FSM

**Swedish:** Analysera vad nedanstående tillståndsmaskin (FSM) utför.

1. Ta fram Boolska uttryck för nästa tillstånd.
2. Rita tillståndstabell.
3. Rita tillståndsdigram.  
Använd ordningen Q2:0

**English:** Analyze the state machine (FSM) below.

1. Derive Boolean expressions for next state.
2. Draw a state table.
3. Draw a state diagram.  
Use the order Q2:0

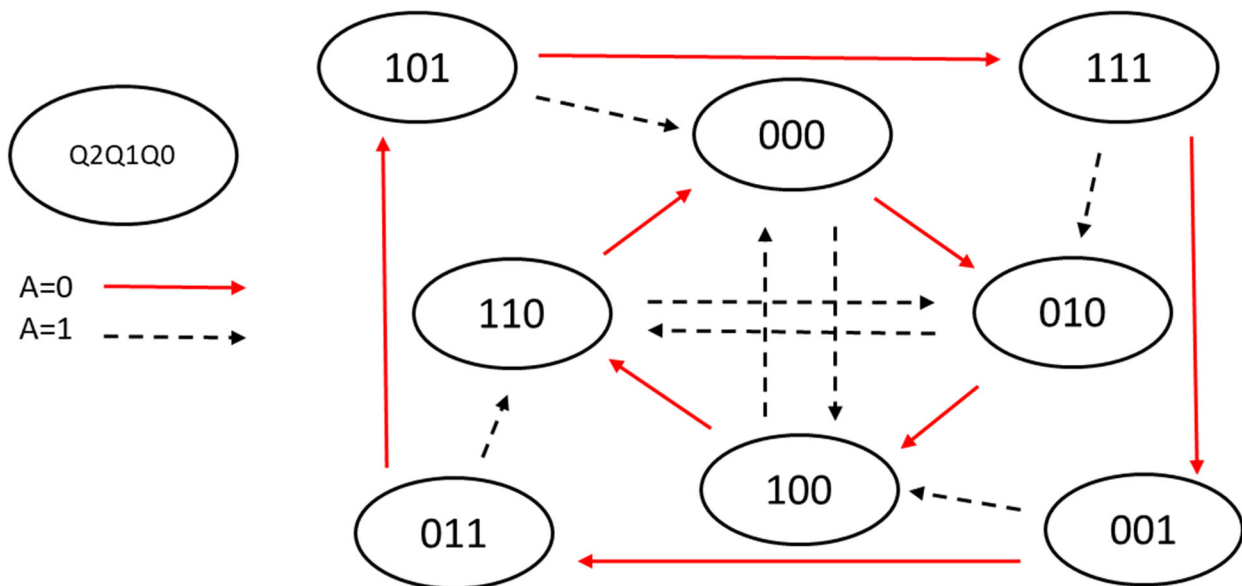


$$Q2+ = \overline{Q2} \cdot Q1 + \overline{A} \cdot Q2 \cdot \overline{Q1} + A \cdot \overline{Q2}$$

$$Q1+ = A \cdot Q1 + \overline{A} \cdot \overline{Q1} = A \oplus Q1$$

$$Q0+ = \overline{A} \cdot Q0$$

Present state			Next state A = 0			Next state A = 1		
Q2	Q1	Q0	Q2+	Q1+	Q0+	Q2+	Q1+	Q0+
0	0	0	0	1	0	1	0	0
0	0	1	0	1	1	1	0	0
0	1	0	1	0	0	1	1	0
0	1	1	1	0	1	1	1	0
1	0	0	1	1	0	0	0	0
1	0	1	1	1	1	0	0	0
1	1	0	0	0	0	0	1	0
1	1	1	0	0	1	0	1	0



If A=0: +2

If A=1: +4 for even and +3 for odd numbers

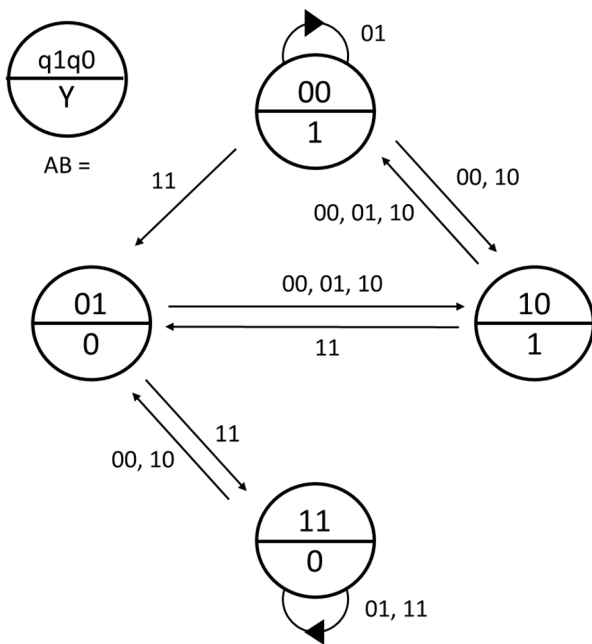
## 20 Design of FSM

**Swedish:** Konstruera en tillståndsmaskin (FSM) enligt tillståndsdigrammet nedan.

1. Rita tillståndstabell.
2. Ta fram K-map för nästa tillstånd.
3. Ta fram minimerade uttryck för nästa tillstånd och utsignal.
4. Rita kretsschema för en FSM med DFFs och vilka grindar som helst.

**English:** Design a state machine (FSM) according to the state diagram below.

1. Draw a state table.
2. Derive K-maps for next states.
3. Derive minimized expressions for next state and output.
4. Draw the FSM circuit diagram with DFFs and any gates.



q1q0 = 00	A B =			
	00	01	11	10
01				
11				
10				

Rita om K-map i dina inlämnade svar.

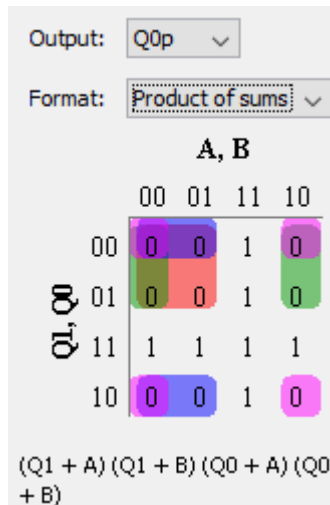
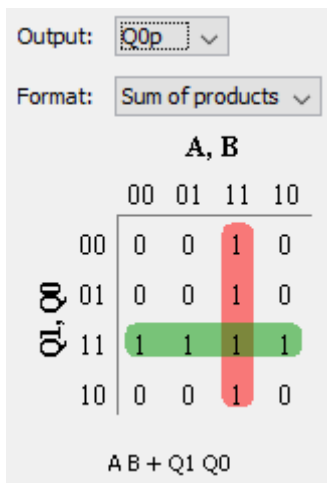
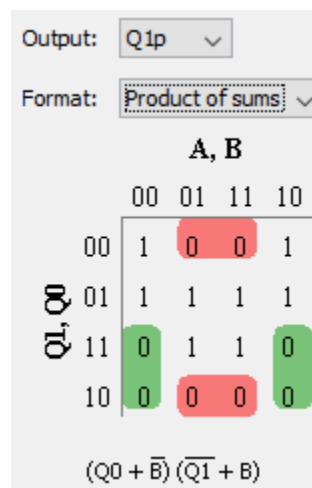
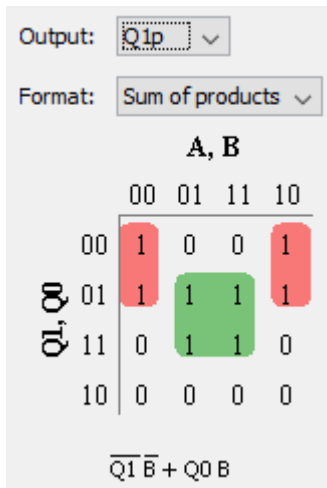
Redraw the K-map in your answer sheets.

Present state		Next state								Out
		AB = 00		AB = 01		AB = 11		AB = 10		
q1	q0	q1+	q0+	q1+	q0+	q1+	q0+	q1+	q0+	Y
0	0	1	0	0	0	0	1	1	0	1
0	1	1	0	1	0	1	1	1	0	0
1	1	0	1	1	1	1	1	0	1	0
1	0	0	0	0	0	0	1	0	0	1

q1+	AB=				
q1q0	00	01	11	10	
00	1	0	0	1	
01	1	1	1	1	
11	0	1	1	0	
10	0	0	0	0	

q0+	AB=				
q1q0	00	01	11	10	
00	0	0	1	0	
01	0	0	1	0	
11	1	1	1	1	
10	0	0	1	0	

K-map not needed for Y,  $Y = \overline{q_0}$   
Continues on next page



$$Y = \overline{q0}$$

