Written exam
IE1204/5 Digital Design
Friday 13/1 2017 08.00-12.00

General Information

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Exam text does not have to be returned when you hand in your writing.

Aids: No aids are allowed!
The exam consists of three parts with a total of 14 tasks, and a total of 30 points:

Part A1 (Analysis) containes ten short questions. Right answer will give you one point. Incorrect answer will give you zero points. The total number of points in Part A1 **is 10 points**. To **pass the Part A1 requires at least 6p**, *if fewer points we will not look at the rest of your exam.*

Part A2 (Methods) contains two method problems on a total of 10 points.

To **pass the exam** requires at least **11 points** from A1 + A2 , *if fewer points we will not look at the rest of your exam.*

Part B (Design problems) contains two design problems of a total of 10 points. Part B is corrected only if there are at **least 11p** from the exam A- Part.

NOTE ! At the end of the exam text there is a submission sheet for Part A1, which shall be separated and be submitted together with the solutions for A2 and B.

For a passing grade (**E**) requires at **least 11 points on the exam**. If exactly 10p from A1(6p)+A2(4p), (FX), completion to (E) will be offered.

Grades   are given as follows:

0 –	11 –	16 –	19 –	22 –	25
F	E	D	C	B	A

The result is expected to be announced before Friday 3/2 2017.

Part A1: Analysis

Only answers are needed in Part A1. Write the answers on the submission sheet for Part A1, which can be found at the end of the exam text.

1. 1p/0p
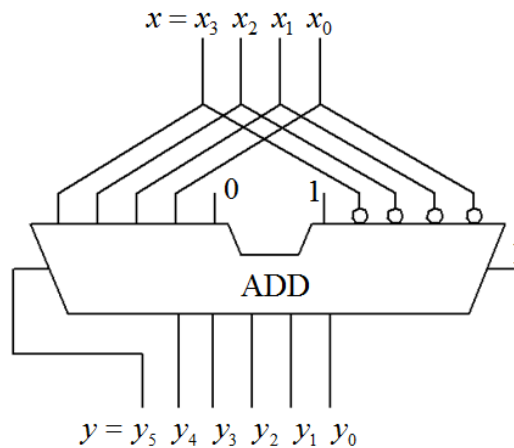A function $f(x, y, z)$ is described on minimized SoP form (Sum of products):
$$f(x, y, z) = \{SoP\}_{min} = y + x \cdot \bar{z}$$
Write down the function as a minimized product of sums.
$$f(x, y, z) = \{PoS\}_{min} = ?$$

2. 1p/0p
Useless circuit (!). A 5-bit adder is connected to multiply a binary unsigned 4-bit number $x = x_3 x_2 x_1 x_0$ with a constant k, $y = k \cdot x$. Let the number x be $x = 1010_2$ then what will the (6 bit) sum $y = y_5 y_4 y_3 y_2 y_1 y_0$ be?

3. 1p/0p
A two's complement 16-bit number is $x_{16} = $ FFFB (hexadecimal). This number will be transfered to a 4-bit register (the number of bits will be reduced and the sign kept). Express this 4-bit number as a decimal number with sign $\pm x_{10} = ?$

4. 1p/0p
Given is a Karnaugh map for a function of four variables $Y = f(x_3, x_2, x_1, x_0)$.
Write the function Y_{min}, as a minimized sum of products, on **SoP** form.
"-" in the map means "don't care".

X_1X_0

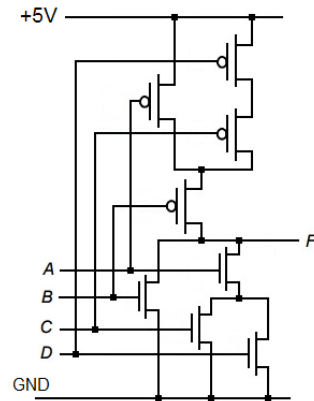| X_3X_2	00	01	11	10
00	^{0}1	^{1}-	^{3}1	^{2}0
01	^{4}-	^{5}1	^{7}1	^{6}0
11	^{12}0	^{13}1	^{15}1	^{14}1
10	^{8}0	^{9}-	^{11}1	^{10}-

5. 1p/0p

The figure below shows a circuit with two NOR gates and two NAND gates. Simplify the function $Y = f(a, b, c, d)$ as much as possible and write the function on SoP-form.
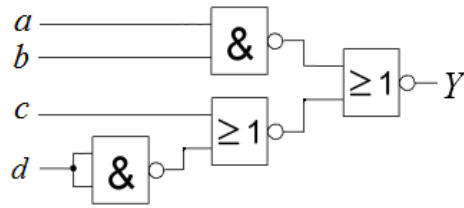
6. 1p/0p

Give an expression for the logical function realized by the CMOS circuit in the figure.

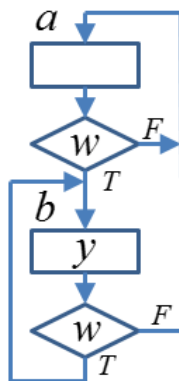Write the function on SoP-form. $F = f(A, B, C, D) = ?$

7. 1p/0p

A State Machine can be drawn either as **state diagram** or as **ASM chart** (Algorithmic State Machine chart).
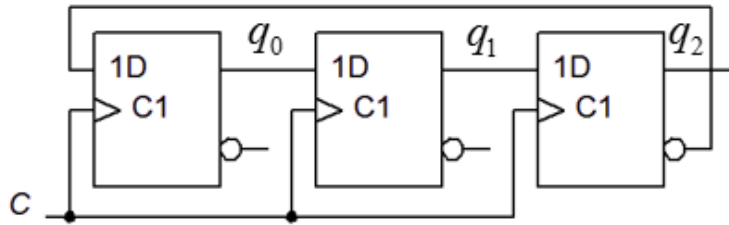
This figure shows an ASM-chart.

Draw the equivalent **Moore state diagram** using the circles in the right figure.
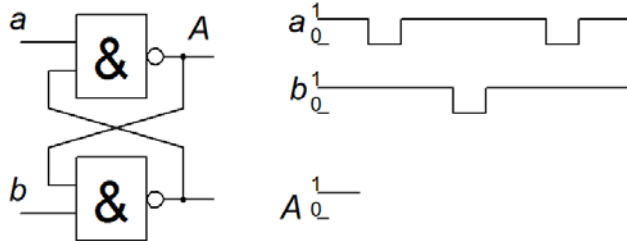
The same figure is also on the submission sheet.

8. 1p/0p

3

A synchronous counter starts in the state $q_2q_1q_0 = 000$. What will the state be after **four** clock pulses? $q_2q_1q_0 = ?$

9. 1p/0p

The figure shows a latch circuit. Complete the timing diagram. The same timing diagram is also on the submission sheet.

10. 1p/0p

At the labs, we use chips from the 74-series. They are nowadays used as spares. These functions can instead be described using VHDL code and downloaded to programmable logic.

The circuit 7421 is shown to the right. Below are the VHDL code for the circuit. In the code, we have hidden the line **o1** from you (with characters ●).
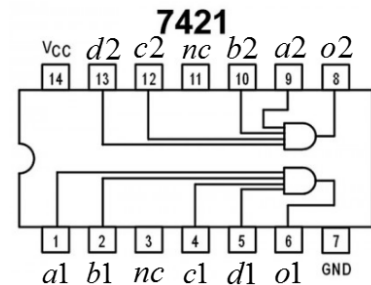
Write VHDL code for the line   **o2 <= ( ) ;**

```
library ieee;
use ieee.std_logic_1164.all;

entity A74XX21 is
   port (
            a1 :  in   std_logic;
            b1 :  in   std_logic;
            c1 :  in   std_logic;
            d1 :  in   std_logic;
            a2 :  in   std_logic;
            b2 :  in   std_logic;
            c2 :  in   std_logic;
            d2 :  in   std_logic;
            o1 :  out std_logic;
            o2 :  out std_logic );
end entity;

architecture dataflow of A74XX21 is
```

```vhdl
begin

    o1 <= (   •• ••• •• ••• •• ••• ••  ) ;

    o2 <= (                            ) ;

end architecture;
```

Part A2: Methods

Note! Part A2 will only be corrected if you have passed part A1 ($\geq 6p$)

11. 4p   **ANDON** signal lights.

In production factories with assembly line a system of warning lights green (G), yellow (Y) and Red (R) are used at the assembly stations. Operators have a stop button (with a cord) that stops the assembly line and all stations then signals **red**. The operator also has an alert button to summon help. It will signal **yellow** light at the own station and for all previous stations along the assembly line, but without stopping it.

When all problems are removed, the assembly line may be started again with a short start pulse (Start). All stations then signals the green light. See the figure that shows three stations with the operator buttons and lights. The arrow indicates the transport direction of the assembly line.
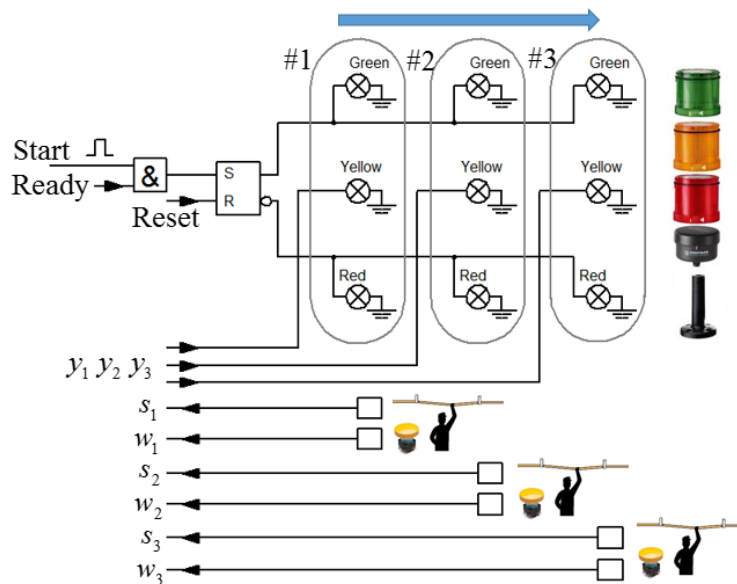
a) (a+b=1p) (**Green**) A short pulse Start = 1 can start the assembly line *if* Ready = 1. Design a circuit that provides signal Ready = 1 if *none* of the stop signals s_1 s_2 s_3 are 1.

b) (**Red**) The assembly line is stopped if Reset =1.

Design a circuit that provides signal Reset = 1 if *any* of the signals s_1 s_2 s_3 is 1.

Reset = $f(s_1, s_2, s_3)$.

Draw the two circuits together, use a few optional gates.

c) (2p) (**Yellow**) Operators can warn on problems by lighting a yellow lamp. The signals w_1 w_2 w_3 shall lit their own yellow light (y_1 at w_1 or y_2 at w_2 or y_3 at w_3), but also lit the yellow lights belonging to the stations that are earlier in the direction of assembly line (stations after shall not be warned).


Set up the truth table for $y_1 y_2 y_3 = f(w_1, w_2, w_3)$.
Derive the functions $y_1 = f(w_1, w_2, w_3)$ $y_2 = f(w_1, w_2, w_3)$ $y_3 = f(w_1, w_2, w_3)$ by inspecting the truth table or by using Karnaugh map. Design the circuit with a few optional gates.
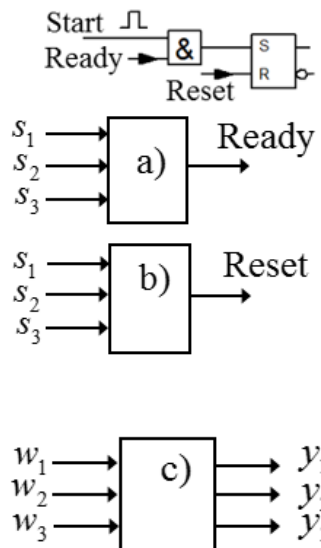
d) (1p) It is common with more than three workstations along a conveyor belt. In the figure, a warning signal w_{IN} *from* an subsequent station, and a warning signal w_{OUT} *to* a previous station, has been added.

Completed the circuit from c) with the signals signal w_{OUT} and w_{IN} in such a way that it works together with the other stations. (Rule: all previous stations must also warn with yellow light).
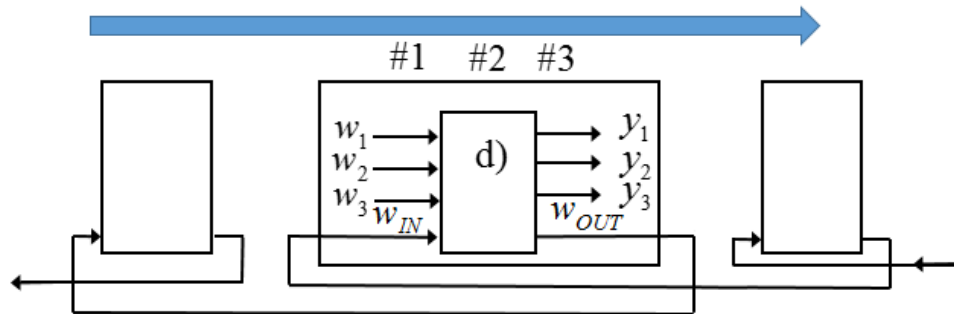
12. 6p Counter.

A modulo-6 synchronous counter consists of three D-flip-flops and one XOR-gate and one AND-gate, se the figure.

a) (1p) Derive the expressions for next state
$q_3^+ = ?$ $q_2^+ = ?$ $q_1^+ = ?$

b) (1p) Set up the complete state table $q_3^+ q_2^+ q_1^+ = f(q_3 q_2 q_1)$

c) (1p) Draw the complete state diagram.

d) (1p) Which states are not part of the modulo-6 sequence? What will happen if one starts from any of these states?
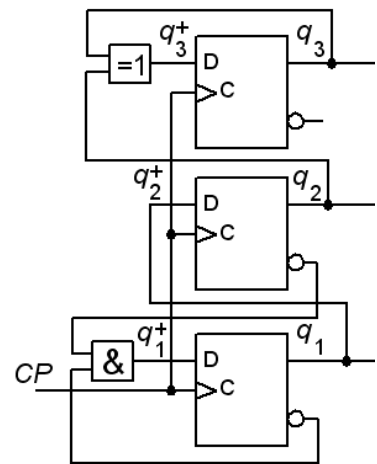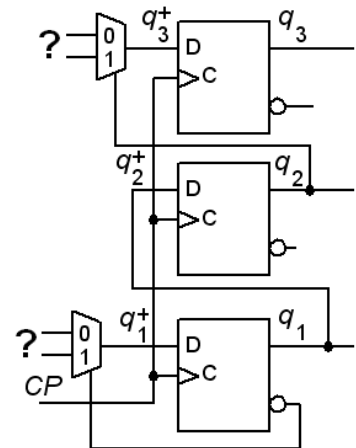

Redesign the circuit, maintaining the function so that it uses **two 2:1 multiplexers** in place of the gates. See figure to the right.

e) (2p) What signals should be connected to the multiplexer data inputs to replace the gates? Motivate answer.

$q_3^+ : mux_0 = ?, \quad mux_1 = ?$

$q_1^+ : mux_0 = ?, \quad mux_1 = ?$

Part B. Design Problems

Note! Part B will only be corrected if you have passed part A1+A2 ($\geq 11p$).

13. 5p Synchronous sequential circuit. Detector for specific event.

A shift register is used to detect when a particular sequence occurs in a sequence of bits to input w. The signal w is synchronized with the clock pulses c. Each time the correct bit sequence appears $z = 1$. At start is $w = 0$.
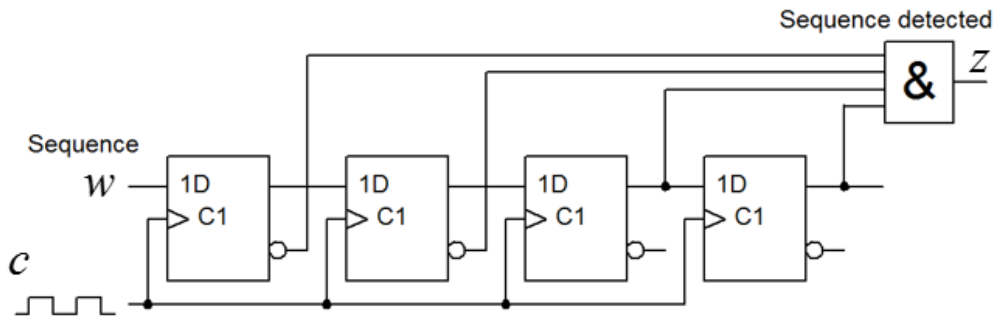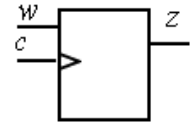

a) (1p) Which bit sequence is detected?

One can construct a Moore machine with fewer D-flip-flops that detects the same sequence.

b) (1p) Draw the **State Diagram** for such a sequence detector.

c) (2p) Derive the **state table** and the **coded state table**, using *binary code* as state code. Derive minimized expressions for **next state decoder** and **output decoder**. You do not need to draw any circuit diagram.

d) (1p) Minimize the following state diagram.
Then draw the minimized **state diagram**.

Note that this is a completely independent task without any connection to the former sequence detector.
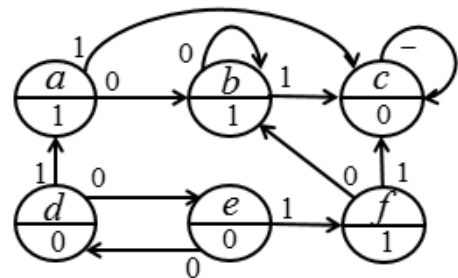
14. 5p Registration of double edges.

Pulses are received at two inputs *a* and *b* of an asynchronous sequential circuit. As soon as a total of two positive edges (transitions from 0→1) has been submitted to the inputs then the output *y* becomes 1 (and then remains 1 regardless of input signals).
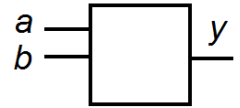
Two edges means that it either enters two pulses to any of the inputs, or enters one pulse to each input. The pulses may come at any time to the inputs and no assumption can be made about the length of the pulses.

At start both input signals are $a = b = 0$. No simultaneous input signal changes can occur.

a) (2p) Study the possible inputs, and set up a proper **flow table** for the sequential circuit. Draw the **state diagram**.

b) (2p) Make a suitable state assignment with an **exitation table** that provides circuits that are free from critical race (comment on how you achieved this). You will also develop the hazard free **expressions** for the **next state** (comment on how you achieved this) as well as an expression for **output**.

c) (0,5p) Draw the circuit diagram. (Use optional gates).

d) (0,5p) To be useful, the sequential circuit will need a Reset input so that it can be re-started. Complete the circuit with such a function. (Use optional gates).
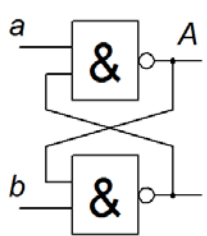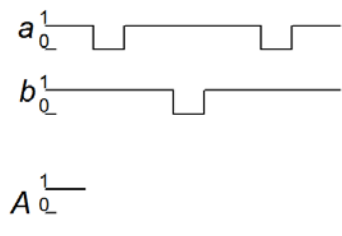
Good Luck!

Submission sheet for Part A1 `Sheet 1`

(remove and hand in together with your answers for part A2 and part B)

Last name: _____   **Given name:** _____

Personal code: _____   **Sheet:**   **1**

Write down your answers for the questions from Part A1 (1 to 10)

Question	Answer
1	$f(x, y, z) = \{PoS\}_{min} = ?$
2	$x = 1010_2 \rightarrow y = k \cdot x = y_5 y_4 y_3 y_2 y_1 y_0 = ?$
3	$x_{16} = \text{FFFB} \rightarrow 4\text{-bit} \rightarrow \pm x_{10} = ?$
4	$Y = \{SoP\}_{min}$
5	$Y = f(a, b, c, d)$
6	$F = f(A, B, C, D)$
7	
8	$q_2 q_1 q_0 = 000 \rightarrow \rightarrow \ \rightarrow \rightarrow ??$
9	
10	`o2 <= (                    ) ;`

This table is completed by the examiner!!

Part A1 (10)	Part A2 (10)		Part B (10)		Total (30)	
Points	11	12	13	14	Sum	Grade