Written exam for
IE1204/5 Digital Design with solutions
Thursday 29/10 2015 9.00-13.00

General Information

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Teacher: William Sandqvist phone 08-7904487

Exam text does not have to be returned when you hand in your writing.

Aids: No aids are allowed!
The exam consists of three parts with a total of 14 tasks, and a total of 30 points:

Part A1 (Analysis) containes ten short questions. Right answer will give you one point. Incorrect answer will give you zero points. The total number of points in Part A1 **is 10 points**. To **pass the Part A1 requires at least 6p**, *if fewer points we will not look at the rest of your exam.*

Part A2 (Methods) contains two method problems on a total of 10 points.

To **pass the exam** requires at least **11 points** from A1 + A2 , *if fewer points we will not look at the rest of your exam.*

Part B (Design problems) contains two design problems of a total of 10 points. Part B is corrected only if there are at **least 11p** from the exam A- Part.

NOTE ! At the end of the exam text there is a submission sheet for Part A1, which shall be separated to be submitted together with the solutions for A2 and B.

For a passing grade (**E**) requires at **least 11 points on the exam**.

Grades are given as follows:

0 –	11 –	16 –	19 –	22 –	25
F	E	D	C	B	A

The result is expected to be announced before Thursday 19/11 2015.

Part A1: Analysis

Only answers are needed in Part A1. Write the answers on the submission sheet for Part A1, which can be found at the end of the exam text.

1. 1p/0p

A function *f*(x, y, z) is described by the expression:

$$f(x,y,z)=\overline{x\cdot y\cdot z}+x\cdot\bar{y}\cdot\bar{z}+\overline{(y+z)}$$

Write down the function maxterms, eg. the function as a product of sums.

$$f(x,y,z)=\{PoS\}=?$$

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1. Proposed solution

$$f(x,y,z)=\overline{x\cdot y\cdot z}+x\cdot\bar{y}\cdot\bar{z}+\overline{(y+z)}=(\bar{x}+\bar{y}+\bar{z})+x\bar{y}\bar{z}+\bar{y}\bar{z}=\bar{x}+\bar{y}+\bar{z}+\bar{y}\bar{z}(x+1)=$$

$$=\bar{x}+\bar{z}+\bar{y}(1+\bar{z})=(\bar{x}+\bar{y}+\bar{z})\quad \text{only one maxterm is needed}$$

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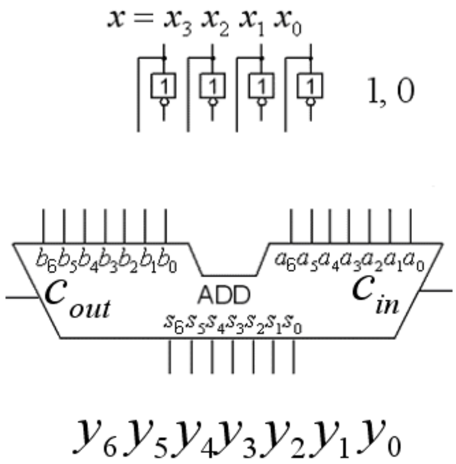
2. 1p/0p

A four bit unsigned integer x ($x_3x_2x_1x_0$) is to be multiplicated by the constant **7**.

This is done by connecting the number x to a seven bit adder that is configured to do the operation

$y = 7\cdot x = (8\cdot x - 1\cdot x)$

Draw how the adder is to be configured. Except the four bits in x there are also bits with the values 0 and 1 if needed. You will find a copy of the figure on the submission sheet.



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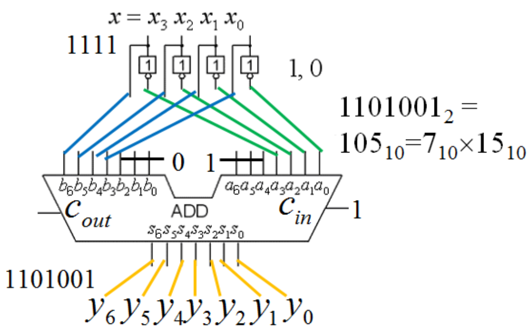
2. Proposed solution $\quad y=7\cdot x=(8\cdot x-1\cdot x)$



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3. 1p/0p

Two binary 6 bit two complement numbers are added. What will the result be expressed as a signed decimal number?

$$\begin{array}{r} 001011 \\ +\ 101110 \\ \hline \end{array} = \text{signed decimal } \pm ??_{10}$$

---

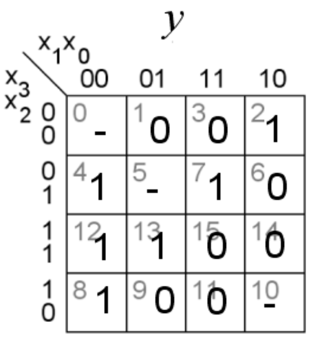
3. Proposed solution $\quad 001011+101110 = 111001 \quad -2^5 + 11001_2 = -32 + 25 = -7$

$$\begin{array}{r} \underline{111} \\ 001011 \\ +\ 101110 \\ \hline 111001 \end{array} = -000111 = -7_{10}$$

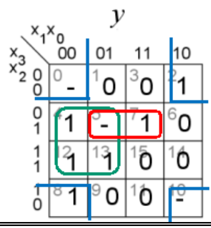
---

4. 1p/0p

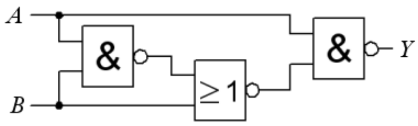
Given is a Karnaugh map for a function of four variables $y = f(x_3, x_2, x_1, x_0)$.
Write the function as a minimized y_{min} sum of products, **SoP** form.
”-” in the map means ”don’t care”.



4. Proposed solution $y = \bar{x}_2\bar{x}_0 + x_2\bar{x}_1 + \bar{x}_3 x_2 x_0$

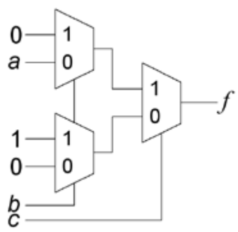


5. 1p/0p
The figure bellow shows a circuit with two NAND gates and one NOR-gate. Simplify the function $Y = f(A, B)$ as much as possible.



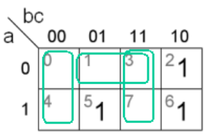
5. Proposed solution
$Y = \overline{A\cdot\overline{A\cdot B + A}} = \bar{A} + A\cdot B + A = 1$

6. 1p/0p
A logic function of three variables $c\ b\ a$ is realized with multiplexors. Write the function on minimized **PoS** form (as a product of sums).



$f(c,b,a) = \{PoS\}_{\min} = ?$

6. Proposed solution
$f(c,b,a) = \{SoP\} = 0\cdot bc + a\cdot\bar{b}c + 1\cdot b\bar{c} + 0\cdot\bar{b}\bar{c} = a\bar{b}c + b\bar{c} = a\bar{b}c + (a+\bar{a})b\bar{c} = a\bar{b}c + ab\bar{c} + \bar{a}b\bar{c}$

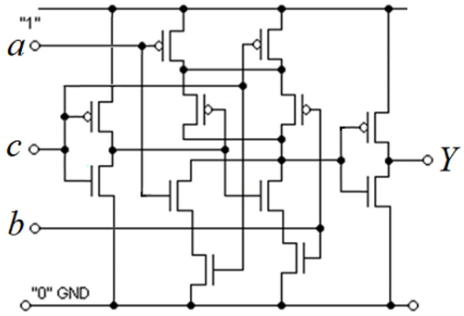


$f(c,b,a) = \{PoS\}_{\min} = (\bar{b}+\bar{c})(b+c)(a+\bar{c}) \quad or \quad = (\bar{b}+\bar{c})(b+c)(a+b)$

7. 1p/0p

Give an expression for the logical function realized by the CMOS circuit in the figure?

$Y = f(a,b,c) = ?$



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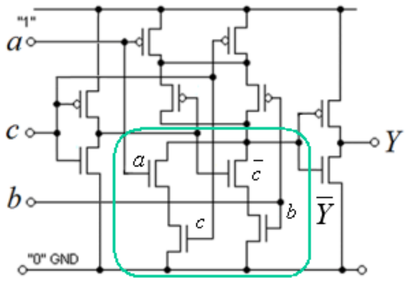
7. Proposed solution



$PDN: \quad \overline{Y} = ac + b\overline{c}$

$\Rightarrow \overline{\overline{Y}} = Y = ac + b\overline{c}$

CMOS Multiplexor

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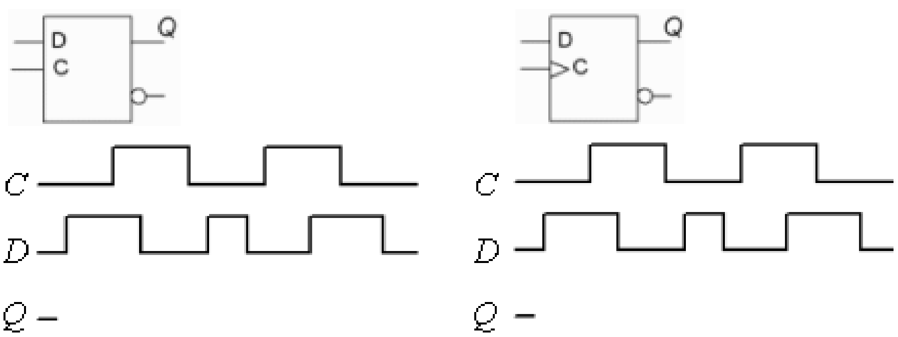
8. 1p/0p



Complete the timing diagram for the D-latch and D-flipflop by drawing signal Q for booth cases. Draw the figure so that it is clear **what** is causing the changes in the Q!

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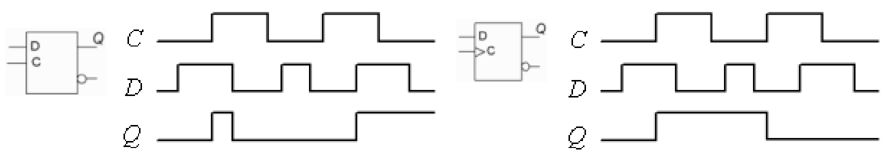
8. Proposed solution



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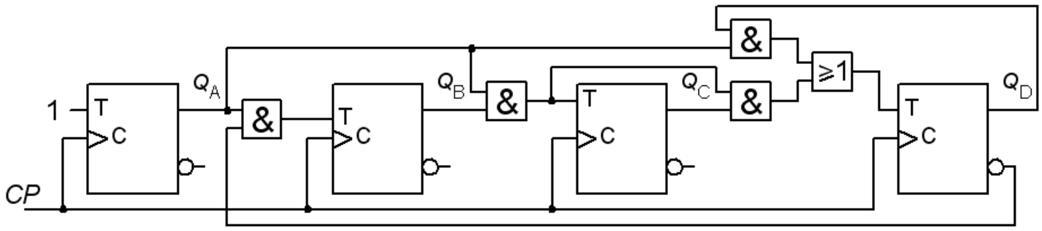
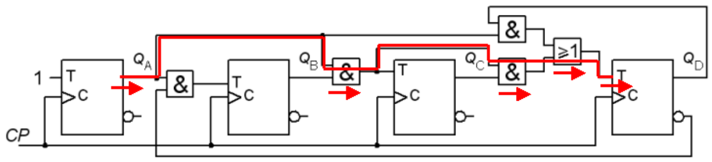
9. 1p/0p



The figure shows a synchronous decade counter ($Q_D Q_C Q_B Q_A$ 0…9). Mark (= draw in the figure on the answer sheet) the **critical path** that determines how fast the counter can count. Calculate the minimum time T [ns] between the clock pulses that still provides safe operation.

Gates: $t_{pdOR} = 4$, $t_{pdAND} = 5$ [ns]   Flip-flops: $t_{su} = 3$, $t_h = 1$, $t_{pdQ} = 2$ [ns]

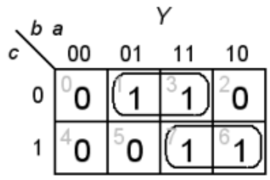
9. proposed solution



$$T = t_{pdQ} + t_{psAND} + t_{psAND} + t_{psOR} + t_{su} =$$
$$= 2 + 5 + 5 + 4 + 3 = 19 \text{ ns}$$

10. 1p/0p

Below is the VHDL code for a 2: 1 multiplexer. The multiplexer Karnaugh map is shown at right. Complete code so that it becomes a **Hazard free** MUX. The line of code is also available on the answer sheet.

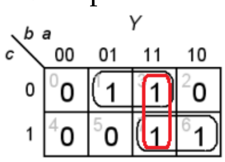



```
-- import std_logic from the IEEE library
library IEEE;
use IEEE.std_logic_1164.all;

-- this is the entity
entity MUX is
  port (
    a  : in std_logic;
    b  : in std_logic;
    c  : in std_logic;
    Y  : out std_logic);
end entity MUX;

-- this is the architecture
architecture gates of MUX is
begin
  Y <= (b AND c) OR (a AND NOT c) [                          ;]
end architecture gates;
```

10. Proposed solution

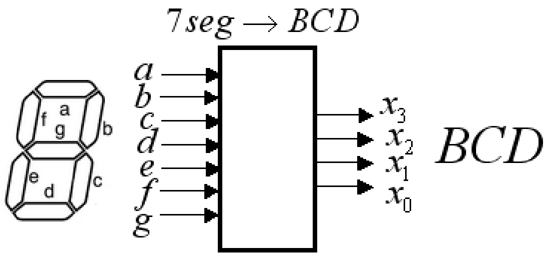


Y <= (b AND c) OR (a AND NOT c) **OR (a AND b);**

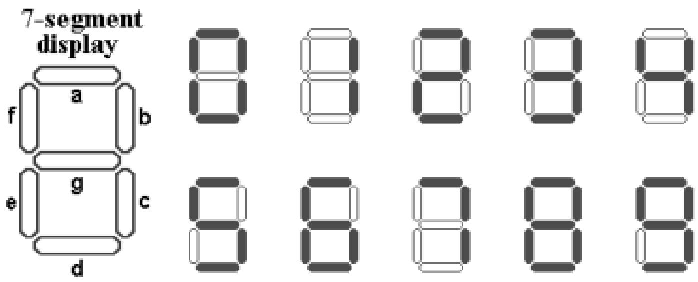
Part A2: Methods

Note! Part A2 will only be corrected if you have passed part A1 ($\geq 6p$)

11. 5p One older instrument has a seven segment display with seven light bulbs, but it lacks an outlet for connection to a computer. One could therefore need a combinatorial circuit that connects to the bulbs and then converts 7-segment code to the usual BCD code (normal binary coded digits 0 to 9) that is used by a variety of other equipments.



a) (1p) Set up the **truth table** for the ten BCD numbers. Black segment is ”1” in figure. $(x_3 x_2 x_1 x_0)_{BCD} = f(abcdefg)$



b) (1p) Inspect the **truth table**. You can discover that even if up to two of the segments are excluded as inputs, the relationship remains distinct between image segments and BCD digits. Find one/two segments that you can do without? Derive the **new truth-table** without this/these segments.

c) (2p) Draw the karnaugh maps for the four BCD-code bits and derive the **minimized expressions** for x_3 x_2 x_1 x_0 in SoP-form. Segment combinations that never occurs should be exploited as don't care. (With the excluded segments in the truth table, the number of variables will be manageable).

d) (1p) Choose yourself one of the expressions x_3 x_2 x_1 x_0 and realize it using only 2 input **NAND** gates. (No inverted variables are available)

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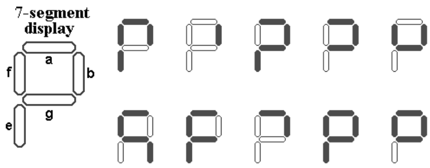
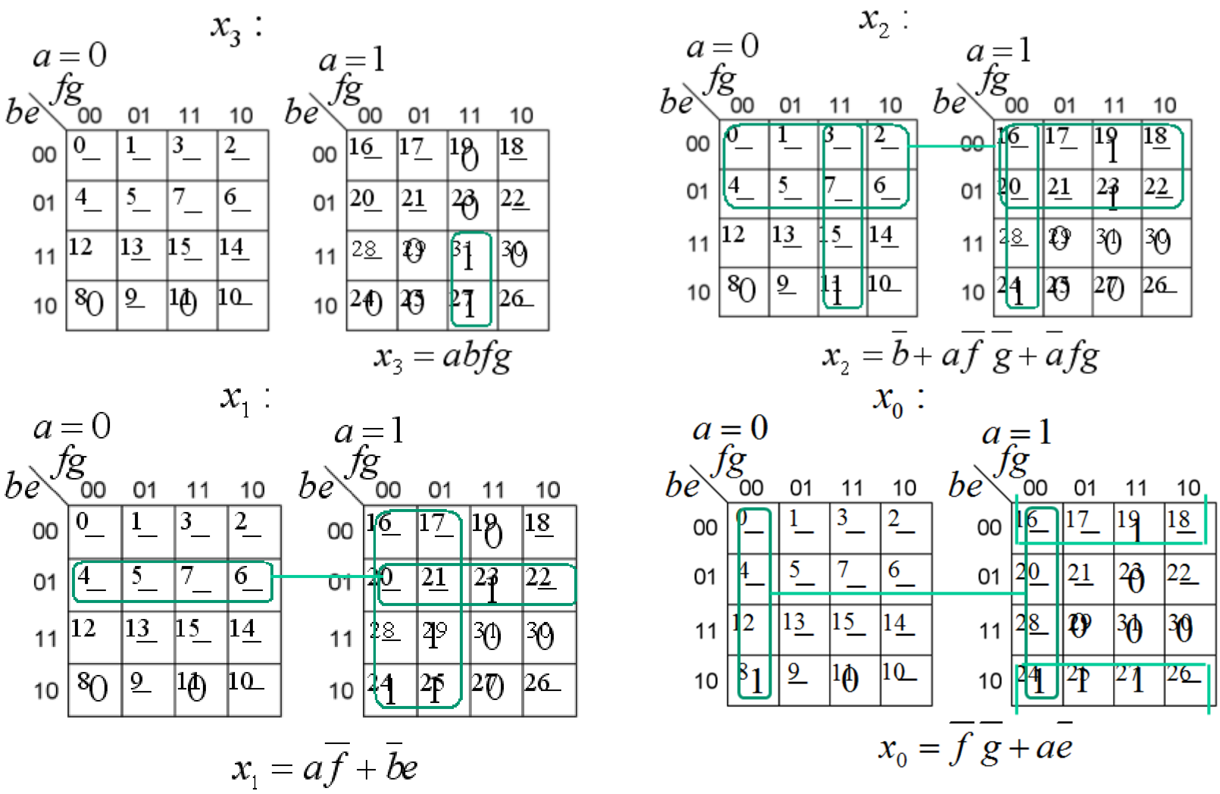
11. Proposed solution

	abcdefg		$x_3x_2x_1x_0$
126	1111110	0	0000
48	0110000	1	0001
109	1101101	2	0010
121	1111001	3	0011
51	0110011	4	0100
91	1011011	5	0101
95	1011111	6	0110
112	1110000	7	0111
127	1111111	8	1000
123	1111011	9	1001



Segment *a* is necessary distinguish between ”1” and ”7”. Segment *e* is needed to distinguish between ”8” from ”9” and ”5” from ”6”. Segments c and d could be excluded without the encoding becoming ambiguous. See the figure. This can be used to simplify the problem down to 5 variables.

	abefg		$x_3x_2x_1x_0$
30	11110	0	0000
8	01000	1	0001
29	11101	2	0010
25	11001	3	0011
11	01011	4	0100
19	10011	5	0101
23	10111	6	0110
24	11000	7	0111
31	11111	8	1000
27	11011	9	1001



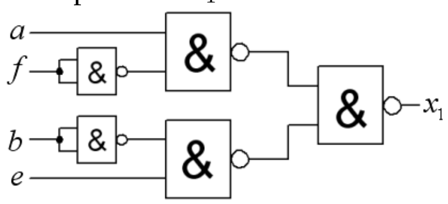
$x_3 = abfg$

$x_2 = \bar{b} + a\bar{f}\,\bar{g} + \bar{a}fg$

$x_1 = a\bar{f} + \bar{b}e$

$x_0 = \bar{f}\,\bar{g} + a\bar{e}$

Example. Bit x_1 :



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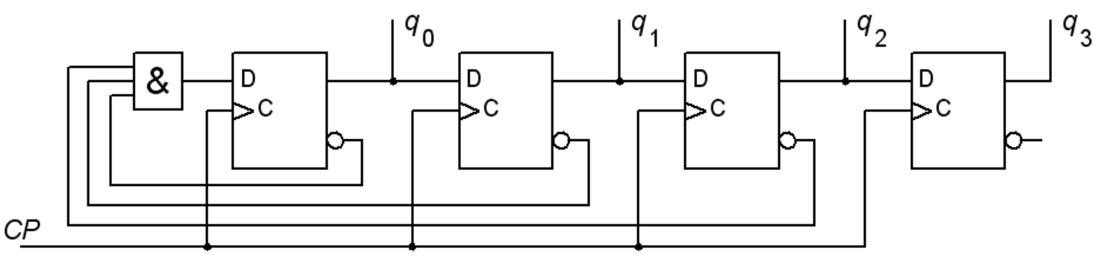
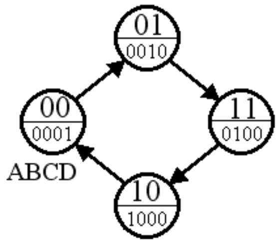
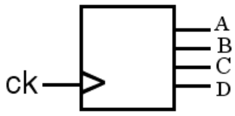
10. 5p The figure shows a "self-correcting ring counter" counting the "one hot" sequence $q_3q_2q_1q_0$ 000**1**, 00**1**0, 0**1**00, **1**000.



a) (2p) Analyze the sequential circuits in the figure and draw the **full state diagram** and the **full state table**. If the counter would start in any other state than any of the four desired "one hot" states, how many clock pulses are required, in the worst case, before the counter has "corrected" this and ends up in the correct sequence?

b) (3p) You can also get the same "one-hot" sequence from a Moore machine with four states, see the state diagram to the right. Derive this sequential circuit with D-flip-flops and optional gates. Use the state encoding from the state diagram. Draw the schematic of the circuit.

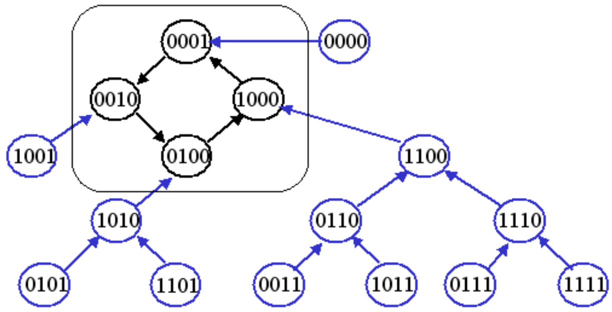




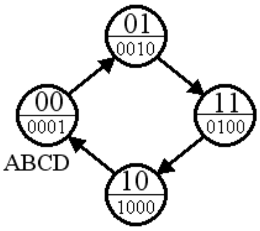
12. Proposed solution

$q_3q_2q_1q_0$	$q_3^+q_2^+q_1^+q_0^+$	$q_3q_2q_1q_0$	$q_3^+q_2^+q_1^+q_0^+$
0000	**0001**	**1000**	**0001**
0001	**0010**	1001	**0010**
0010	**0100**	1010	**0100**
0011	0110	1011	0110
0100	**1000**	1100	**1000**
0101	1010	1101	1010
0110	1100	1110	1100
0111	1110	1111	1110

$q_3^+q_2^+q_1^+q_0^+ = q_2q_1q_0d_0 \quad d_0 = \overline{q_2}\cdot\overline{q_1}\cdot\overline{q_0}$



After at most three clock pulses the "one hot" sequency will be reached!



Q_1Q_0	$Q_1^+Q_0^+$
00	01
01	11
11	10
10	00

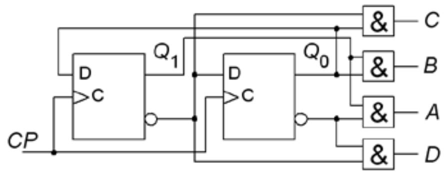
Inspection of table gives:

$Q_1^+ = Q_0 \quad Q_0^+ = \overline{Q}_1$

Decoding:

$A = Q_1\overline{Q}_0 \quad B = Q_1Q_0$

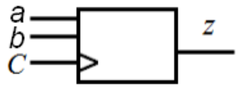
$C = \overline{Q}_1Q_0 \quad D = \overline{Q}_1\overline{Q}_0$



Part B. Design Problems

Note! Part B will only be corrected if you have passed part A1+A2 (≥11p).

13. 4p Sequence Detector. Different inputs three in a row.



You will design a synchronous sequential circuit, in the form of a positive edge-triggered Moore machine with D flip-flops. The input signals ***a*** and ***b*** are synchronized with the clock pulses ***C***. The output signal ***z*** will be 1 when ***a*** and ***b*** are different in at least three consecutive clock pulse intervals. For other sequences ***z*** must be equal to 0.

a) (2p) Derive the circuit **state table** and draw the **state diagram**.

b) (1p) Use the Gray code to encode the states and derive the **encoded state table**. Derive the minimized expressions for **next state** and for the **output**.
c) (1p) Draw the **next state decoder circuit**, there is only access to AND, OR, and XOR gates.

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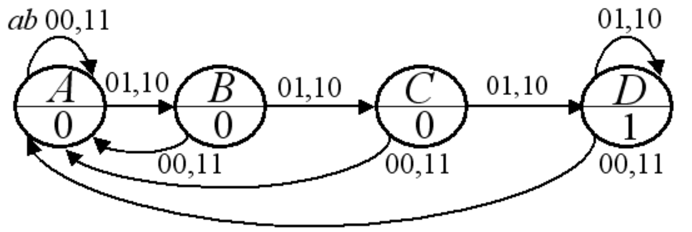
13. Proposed solution



q_1q_0 \ ab	00	01	11	10
$A:00$	$A:00$	$B:01$	$A:00$	$B:01$
$B:01$	$A:00$	$C:11$	$A:00$	$C:11$
$C:11$	$A:00$	$D:10$	$A:00$	$D:10$
$D:10$	$A:00$	$D:00$	$A:00$	$D:00$

$q_1^+q_0^+$

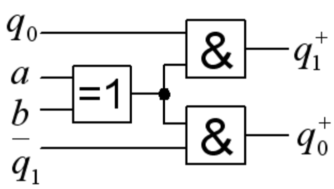
$z = q_1\bar{q}_0$

q_1q_0 \ ab	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	0	1	0	1
10	0	0	0	0

$q_1^+ = q_0(a\bar{b} + \bar{a}b) =$
$= q_0(a \oplus b)$

q_1q_0 \ ab	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	0	0	0
10	0	0	0	0

$q_0^+ = q_1(a\bar{b} + \bar{a}b) =$
$= \bar{q}_1(a \oplus b)$



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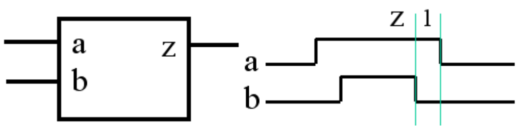
14. 6p Inside pulse detector.

A synchronous sequential circuits "Compares" pulses received on two inputs **a** and **b**. The pulse at the **b** input is always a little shorter than the pulse of **a**, and there will be at most one **b**-pulse during the interval **a**. **b**-pulses will arrive randomly relative to the **a**-pulse. (There are no **exact** simultaneous events).



Sequence circuit must indicate the case when **b** is started (becomes one) after a has started (become one), and **b** has finished (become 0) before **a** finish (become 0). The output **z** will then be = 1 from **b**'s trailing edge to **a**'s trailing edge. **z** must be 0 for all other cases. See the figure time diagram illustrating this case.

a) First, set up a proper **flow table** for the sequence circuit. You don't need from the beginning to care about minimizing the number of states. All positions in the table that can not occur should be treated as don't care.

b) **Simplify the state diagram** by combining compatible state. (Hint. Various solutions are possible, there is among them a solution with four states).

c) Do a suitable **state assignement** with an exitation table which gives a circuit that is **free of critical race**. (Hint. Various solutions are possible, there is a solution with two state variables exploiting unstable transition states and uncritical race).

You should also derive **hazard free expressions** for the next state and an **expression for output**, and draw the **circuits** with the use of optional gates.

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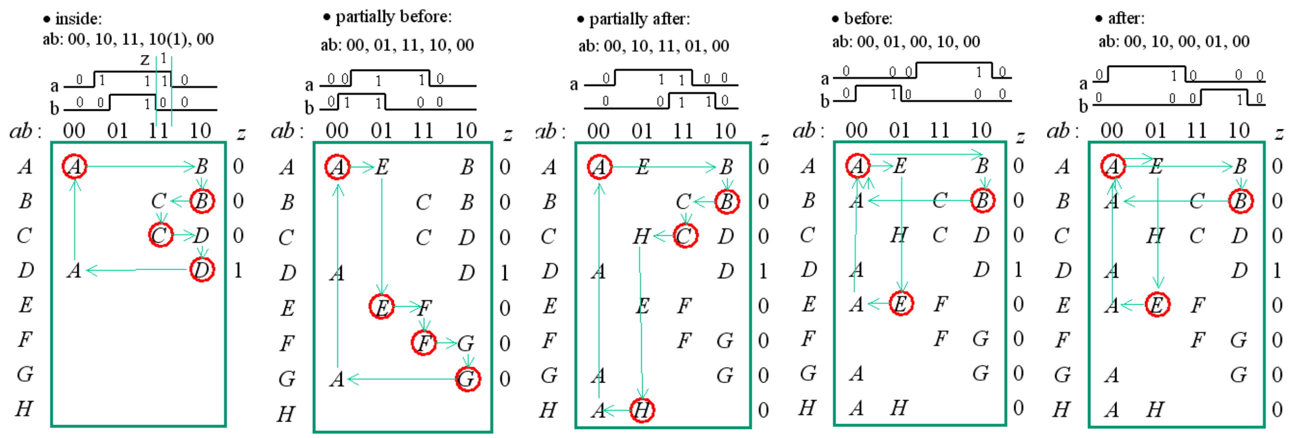
13. Proposed solution – derive state chart step by step



ab:	00	01	11	10	z
A	(A)	E	–	B	0
B	A	–	C	(B)	0
C	–	H	(C)	D	0
D	A	–	*	(D)	1
E	A	(E)	F	–	0
F	–	*	(F)	G	0
G	A	–	*	(G)	0
H	A	(H)	*	–	0

ab:	00	01	11	10	z
A	(A)	E	–	B	0
B	A	–	C	(B)	0
C	–	H	(C)	D	0
D	A	–	–	(D)	1
E	A	(E)	F	–	0
F	–	–	(F)	G	0
G	A	–	–	(G)	0
H	A	(H)	–	–	0

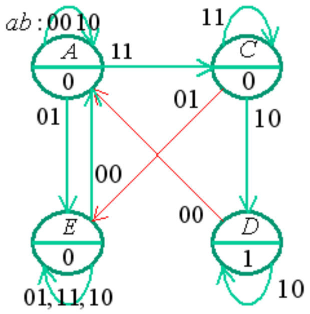
(EFGH)=E

ab:	00	01	11	10	z
A	(A)	E	–	B	0
B	A	–	C	(B)	0
C	–	E	(C)	D	0
D	A	–	–	(D)	1
E	A	(E)	(E)	(E)	0

(AB)=A

ab:	00	01	11	10	z
A	(A)	E	C	(A)	0
C	–	E	(C)	D	0
D	A	–	–	(D)	1
E	A	(E)	(E)	(E)	0

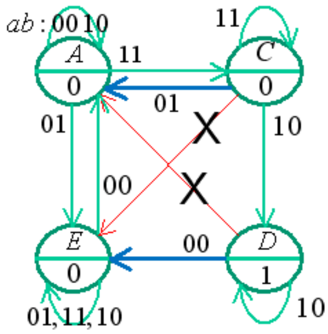
- can not occur, double change in input
* has not occurred in any of the possible sequences, then will not occur



A:00 C:01 D:11 E:10

ab:	00	01	11	10	z
A	A	E	C	A	0
C	–	~~E~~ A	C	D	0
D	~~A~~ E	–	–	D	1
E	A	E	E	E	0

Remove intersecting lines by inserting transition states to avoid hamming distance 2.



ab:	00	01	11	10	z
A	A	E	C	A	0
C	–	A	C	D	0
D	E	–	–	D	1
E	A	E	E	E	0

$z = y_1 y_0$

$Y_1 Y_0 = f(y_1 y_0, a, b)$

y_1y_0 \ ab:	00	01	11	10	z
00	00	10	01	00	0
01	–	00	01	11	0
11	10	–	–	11	1
10	00	10	10	10	0

y_1y_0 \ ab:	00	01	11	10
00	0	1	0	0
01	–	0	0	1
11	1	–	–	1
10	0	1	1	1

$Y_1 = y_0 \bar{b} + y_1 a + y_1 b + \bar{a} b \bar{y}_0$

$y_1 b$ = Hazard cover

y_1y_0 \ ab:	00	01	11	10
00	0	0	1	0
01	–	0	1	1
11	0	–	–	1
10	0	0	0	0

$Y_0 = y_0 a + a b \bar{y}_1$

Good Luck!

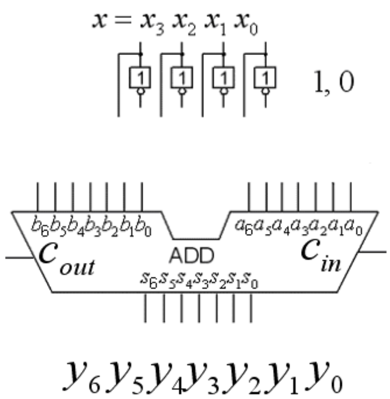
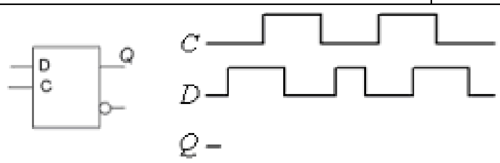
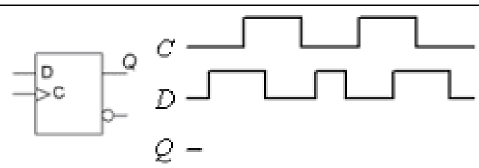
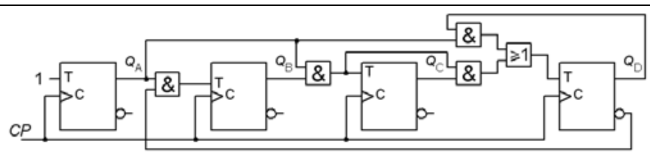
Submission sheet for Part A1 **Sheet 1**

(remove and hand in together with your answers for part A2 and part B)

Last name: ______________________ **Given name:** ______________________

Personal code: ______________________ **Sheet:** **1**

Write down your answers for the questions from Part A1 (1 to 10)

Question	Answer		
1	$f(x,y,z) = \{PoS\} = ?$		
2	$y = 7 \cdot x = (8 \cdot x - 1 \cdot x)$ 	**3**	Signed decimal $\pm??_{10}$ =
4	$f(x_3,x_2,x_1,x_0) = \{SoP\}_{min} = ?$	**5**	$Y = f(A,B) = ?$
6	$f(c,b,a) = \{PoS\}_{min} = ?$	**7**	$Y = f(a,b,c) = ?$
8	 		
9			T [ns] =
10	`Y <= (b AND c) OR (a AND NOT c)` \[; \]		

This table is completed by the examiner!!

Part A1 (10)	**Part A2** (10)		**Part B** (10)		**Total** (30)	
Poäng	11	12	13	14	Sum	Grade