# Exercises 3
Logic Design

Computer Organization and Components / Datorteknik och komponenter (IS1500), 9 hp
Computer Hardware Engineering / Datorteknik, grundkurs (IS1200), 7.5 hp

KTH Royal Institute of Technology
Friday 2nd October, 2015

Gates and Boolean Algebra

1. Draw the symbols and write out the truth tables for the following logic gates:
   AND, OR, NOT, NAND, NOR, XOR

2. Consider the circuit below:
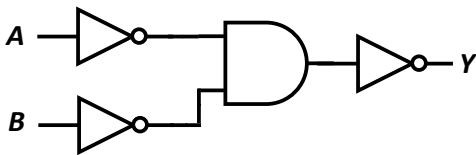
   (a) Create the truth table for the circuit.

   (b) Write down the corresponding boolean algebra expression.

   (c) Simplify the circuit. Explain which boolean algebra theorems that are used.

3. The following circuit includes a tristate buffer:
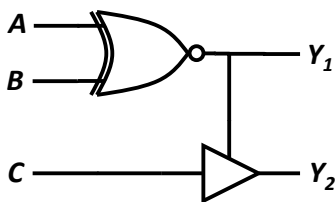
   (a) Create the truth table for the circuit

   (b) Explain what the tristate buffer is doing and what the output from the buffer means.

4. Consider the following truth table.

S	A	B	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

   (a) Create the corresponding boolean expression in sum-of-products form.

   (b) Simplify the expression using the boolean theorems presented at Lecture 7. Clearly state which theorems that you are using.

   (c) Draw the final circuit in a simple form, that is, reuse as many gates as possible.

Multiplexers, Decoders, and Adders

5. The following tasks concerns a 2:1 multiplexer.

   (a) Draw the symbol for the multiplexer.

   (b) Create the truth table in a short form, where the "don't care" symbol "?" is used as often as possible.

   (c) Draw a circuit that gives the same meaning as the above 2:1 multiplexer. The circuit should consist of exactly 2 AND-gates, 1 OR-gate, and 1 NOT-gate.

   (d) How does this circuit compare to the solution of exercise 4c.

6. Decoders.

   (a) Draw a figure for a 3:8 decoder.

   (b) Write out the truth table for a 2:4 decoder.

   (c) Explain the meaning of the numbers that determine the size of the two encoders 3:8 and 2:4.

   (d) Create a circuit consisting of AND-gates, OR-gates, and NOT-gates that defines a 2:4 decoder.

7. Assume that you want to create a 4:1 multiplex where the data input/output ports have 8-bit bus width. Draw the multiplexer. Note that you must clearly show the bus width of the wires.

8. Construct a circuit that takes a 6-bit input A and outputs a 6-bit signal Y, where the output is A multiplied by value 3. You should use 1-bit full adders and basic gates.

9. Construct a 4-bit equality comparator that checks that two input signals A and B are equal, that is, that each corresponding bit has the same value.

## Latches, Flip-Flops, Registers, and Register Files

10. The following figure shows a SR latch.
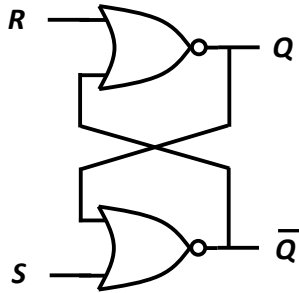
Construct the truth table for the SR latch, by considering each possible input. Explain how and why the signals stabalize for each possible input.

11. D Flip-Flops

    (a) Draw the symbol for a D Flip-Flop with enable signal.

    (b) Explain what the D Flip-Flop above means and in what way it is different from SR latches and D latches.

    (c) Consider the clock signals below. Assume that the D Flip-flop is activated on the rising edge. Draw the output signal Q. Assume that Q is 0 at the beginning of the example sequence.
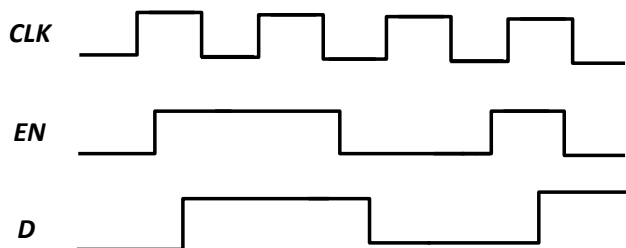
12. Consider the following circuit where the register is triggered on the rising clock edge.
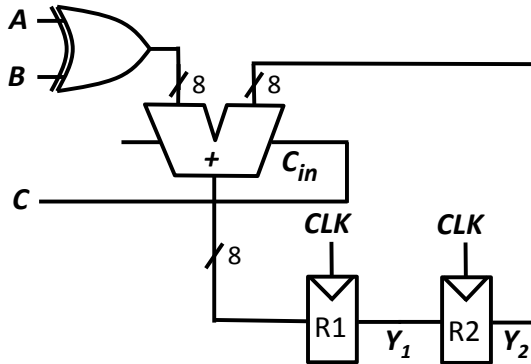
(a) Assume that register R1 holds value 0x3, register R2 value 0x5, $A = 3$, $B = 0$, and $C = 0$. Show the signal values for signals Y_1 and Y_2 for the first 3 clock cycles.

(b) Assume that register R1 holds value 0x10, register R2 value 0x8, $A = 2$, $B = 255$, and $C = 1$. Show the signal values for signals Y_1 and Y_2 for the first 3 clock cycles.

13. Consider the following register file. Assume that $N = 4$ and $M = 16$.
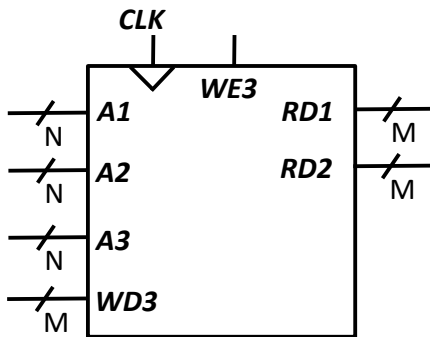
(a) What is the difference between a register file and a register?

(b) How many ports has the above the register file got? How many input ports and how many output ports?

(c) What is the total number of bits of data that this register file can store?

(d) Assume the following mapping from addresses to memory values $\{0\text{x}3 \mapsto 0\text{x}3\text{f}$, $0\text{xa} \mapsto 0\text{x}22, 0\text{x}9 \mapsto 0\text{xe}7\}$ is a known state of the register file. Assume further that $A_1 = 0\text{xa}$, $A_2 = 0\text{x}9$, $A_3 = 0\text{x}3$, $WD_3 = 0\text{x}53$, and $WE_3 = 0\text{x}1$. What are then the values for RD_1 and RD_2 and what is the new known state of the register file?