KTH Information and Communication Technology

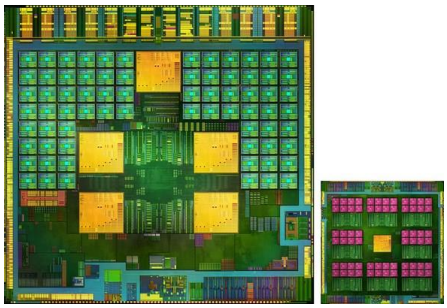
March 22, 2015

IS2202, Computer systems architecture

Course PM 2015

Aim and goal

Computer architecture has never been more exciting than now. Much of the conventional wisdom now turns out to be highly questionable. Transistors used to be expensive and power free. The opposite now holds. We used to believe that higher performance could be achieved by increasing the utilization of instruction-level-parallelism, ILP, using clever compilers, a lot of hardware, speculative execution etc. In real life, we get very little return from these efforts. Uniprocessors used to get twice the performance every 1.5 years. Now the time to double the performance may be as long as 5 years. The current trend is instead to make use of thread-level parallelism, or request-level parallelism at a grander scale, and all computer system designs, from embedded systems, through desk-top computers to high-end compute servers are now *multiprocessors*, computers that work with multiple processor cores. The introduction of multicore processors in desk-top computers has also given rise to a need for programmers that can expose the parallelism in the applications the computers are used for. The figure below shows the NVIDIA Tegra 4. A multicore processor from the NVIDIA containing four ARM Cortex-A15 cores, one ARM 7 core and a 72-core GeForce GPU. Such complicated asymmetric processor designs are the trend now, and programming these is turning out to be the grandest challenge



In this course, you will learn about existing, past and possibly future computer systems, their design and architecture. The overall objective with the course is to give knowledge and insights into the design of modern computers, in particular the processor design including parallel computational pipelines and advanced memory hierarchies.

Starting from this year, the course mixes on-line interactive lectures with in-class lectures which have focus on review of difficult material and problem solving. There are homework assignments which will give bonus towards exam and laboratory exercises where you study computer architectures through simulation.

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Teachers

Course responsible and examiner:

Professor Mats Brorsson, email: matsbror@kth.se, room: 8527 at KTH *School of Information and Communication Technology*, ICT.
Tel. 08-790 41 21.

Office hours: no, talk to me by Skype: matsbror

Other teachers:

Johnny Öberg, email: johnnyob@kth.se

Christian Schulte, email: schulte@kth.se

Literature

The following textbook is required reading:

Computer Architecture: A quantitative approach, 5th ed.
by John Hennessy and David Patterson
Morgan Kaufmann, 2012
ISBN: 978-0-12-383872-8

The book is sold at the student union book-store at KTH (Campus Kista). Previous editions are available as ebook at KTH library.

Additional texts may be used and distributed from the course web site at KTH Social.

Course web sites

The course web site is at KTH Social: http://www.kth.se/social/course/IS2202. This site collects all other information needed. The site scalable-learning.com is used for the interactive on-line lectures. Enroll at: http://www.scalable-learning.com/#/users/student with Enrollment Key **905f2bdaf6**.

Examination

The course is graded A-F where E is the lowest passing grade.

The examination is based on a set of home laboratory exercises (performed in groups of maximum two students) and a final exam. The laboratory exercises and the exam are individually graded A-E and the final grade is calculated as a weighted average between the lab (weight 0.47) and the exam (weight 0.53). In this calculation the following grade equivalents are used: A=5, B=4.5, C=4, D=3.5, and E=3. The average is rounded up or down to the nearest grade (e.g. average 3.7 gives grade D and 3.8 grade C).

Students and teachers are expected to abide by the students rights and responsibilities which can be found here: http://www.kth.se/en/student/studentliv/studentratt/studentratt-1.307449.

Exam

The exam consists of two parts. Both are closed book (no aids except dictionaries and writing material are permitted). Part A can give grade E and Part B can if Part A is passed give higher grades D to A.

Part A consists of six problems and five of these have to be solved more or less correct for a passing grade. Bonus points (see below) may exempt you from the need to solve one or more (up to six) problems on part A which will give you more time for Part B.

Part B will only be corrected if you have reached a passing grade, either from Part A, from bonus points or a combination of both. Part B consists of four problems. Each correctly solved problem

corresponds to a higher exam grade. For example, one correctly solved problem on Part B will lead to grade D, three correctly solved problem leads to grade B etc.

Note. Register for the exam on Daisy https://daisy.ict.kth.se at least two weeks before the exam. Students who have not registered may be denied entry to the exam.

A student who has completed the laboratory exercises before the exam and who have passed only four out of the six problems of part A will get grade Fx and is entitled to make a complementing exam to achieve a passing grade (E). This will take place in June 2014.

Laboratory exercises

The course has two laboratory exercises with written reports. These laboratory exercises are done individually and carried out using computer system simulations. Each laboratory exercise is documented in a report and each student will also need to peer review other students' lab reports as part of the examination.

Instructions on how to carry out the labs will be given on the course web.

Bonus points

Students can collect bonus points from active participation in class (taken by attendance) and through the submission and peer review of written homework assignments.

There will be four homework assignments. Each assignment can give one (1) bonus point for a total of four bonus points. *It is required that you finish the interactive on-line lectures on-time (each one has a deadline) to be eligible for the assignment bonus points!*

There are 17 scheduled classroom lectures. With the exception of the first one, during these lecture, the on-line material will be reviewed and students will work on problems to solve. The typical format is 30 minute review, 40-50 minutes group work on problems and 10-20 minutes review of the problems.

Each classroom lecture attended will give 1/7 bonus point but the total maximum is 2 bonus points.

In total, a student can gain six bonus points which will each be credited towards a problem on Part A of the exam. The exact number of points and which problem they correspond to will be given the students before the exam.

Tentative course schedule

See schedule at course web site for rooms of each lecture and exercise sessions.

Below you can see approximately what will be covered on each lecture/exercise.

Lecture #	When	Subject	Bonus?	Literature
1	March 23	Introduction, Fundamentals of Computer Design	X	Ch 1
2	March 25	On-line lecture: review of fundamentals		
3	March 30	On-line lecture: Cache memories and Virtual memory	X	Ch 2
4	March 31	On-line lecture on SW Optimizations. IRL: Review of Caches and SW Optimization, Problem solving	X	Ch 2
5	April 1	On-line lecture on Cache coherence. IRL: review of Cache coherence and Problem solving	X	Ch 5.1-5.3
6	April 13	On-line lecture on Memory models. IRL: review of memory models and problem solving.	X	Ch 5.6
7	April 15	On-line lecture on coherent buses and scalable synchronization. IRL: Review and Problem solving	X	Ch 5.5
8	April 17	On-line lecture on Scalable coherence. IRL: review and problem solving.	X	Ch 5.4
9	April 20	Online lecture on MP programming. IRL Review and problem solving	X	TBD
10	April 22	On-line lecture on CPU and pipelining. IRL: Review and problem solving.	X	Ch 3
11	April 27	Online lecture on optimizations of CPU:s. IRL: Review and problem solving	X	Ch 3
12	April 29	Online lecture on x86 & VLIW. IRL: review and problem solving	X	Ch 3, App H
13	May 4	Online lecture on GPGPUs. IRL: Review and problem solving	X	Ch 4
14	May 6	The datacentre as computer	X	Ch 6
15	May 11	Research problems and thesis opportunities	X	
16	May 13	The HiPEAC Roadmap and looking ahead	X	HiPEAC Roadmap

A few lectures and exercises may need to be moved as compared to the posted schedule so look out for changes.

Welcome to the course!

Mats Brorsson, examiner

Professor of computer architecture