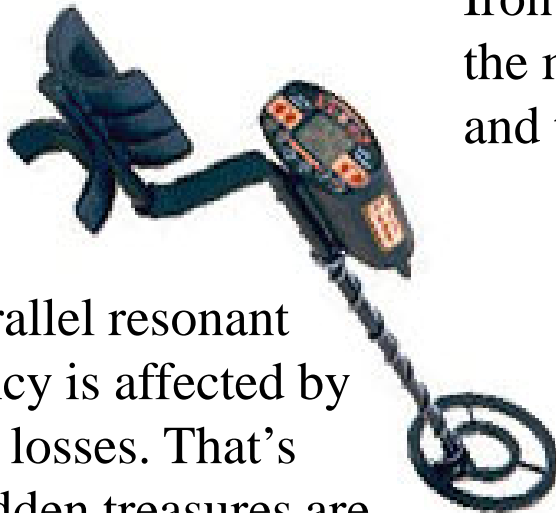


# Metal Detector

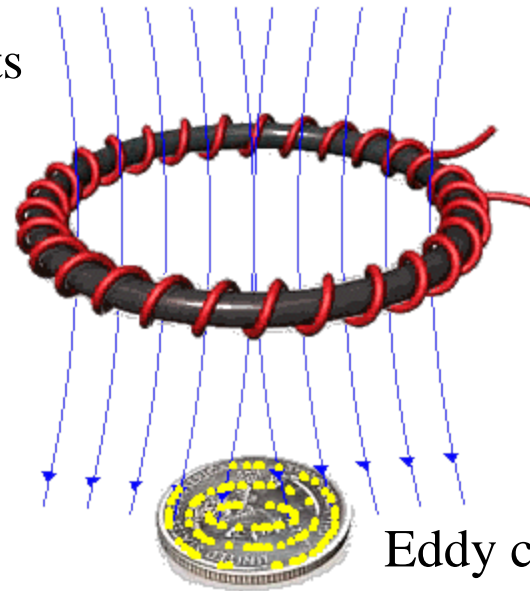
$$f_0 = \frac{1}{2\pi} \sqrt{\left( \frac{1}{LC} - \frac{r^2}{L^2} \right)}$$

Any "losses" (even eddy-current losses in all kinds of metals) are summarized by the symbol  $r$  !

Iron objects affects the magnetic field and thus also  $L$  !



The parallel resonant frequency is affected by the coil losses. That's how hidden treasures are found!



Eddy current losses

# Metal Detector



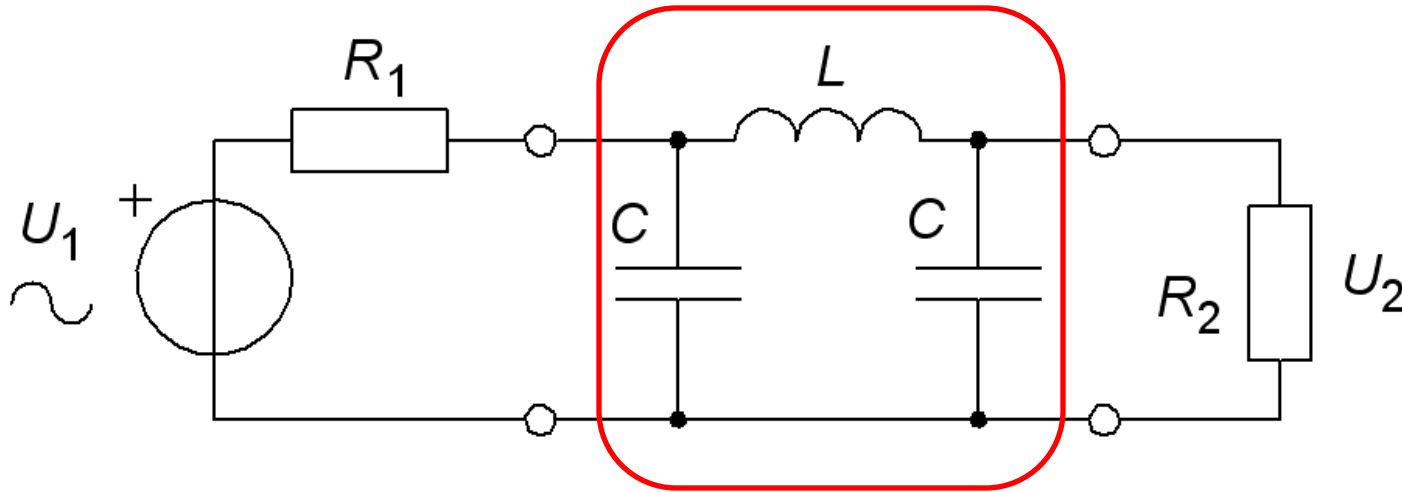
A metal detector consists of an oscillator (a transmitter) with an LC resonant circuit. Metal objects that are within the magnetic field of inductance affects the resonance frequency so that the oscillator frequency changes.

A microprocessor with a frequency measurement program indicates the frequency changes.

- Ahead of the lab, we now need to study resonant circuits and amplifiers – oscillators.

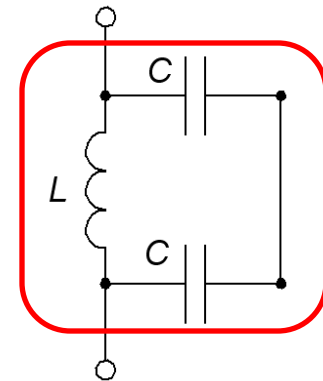
# A circuit with resonance

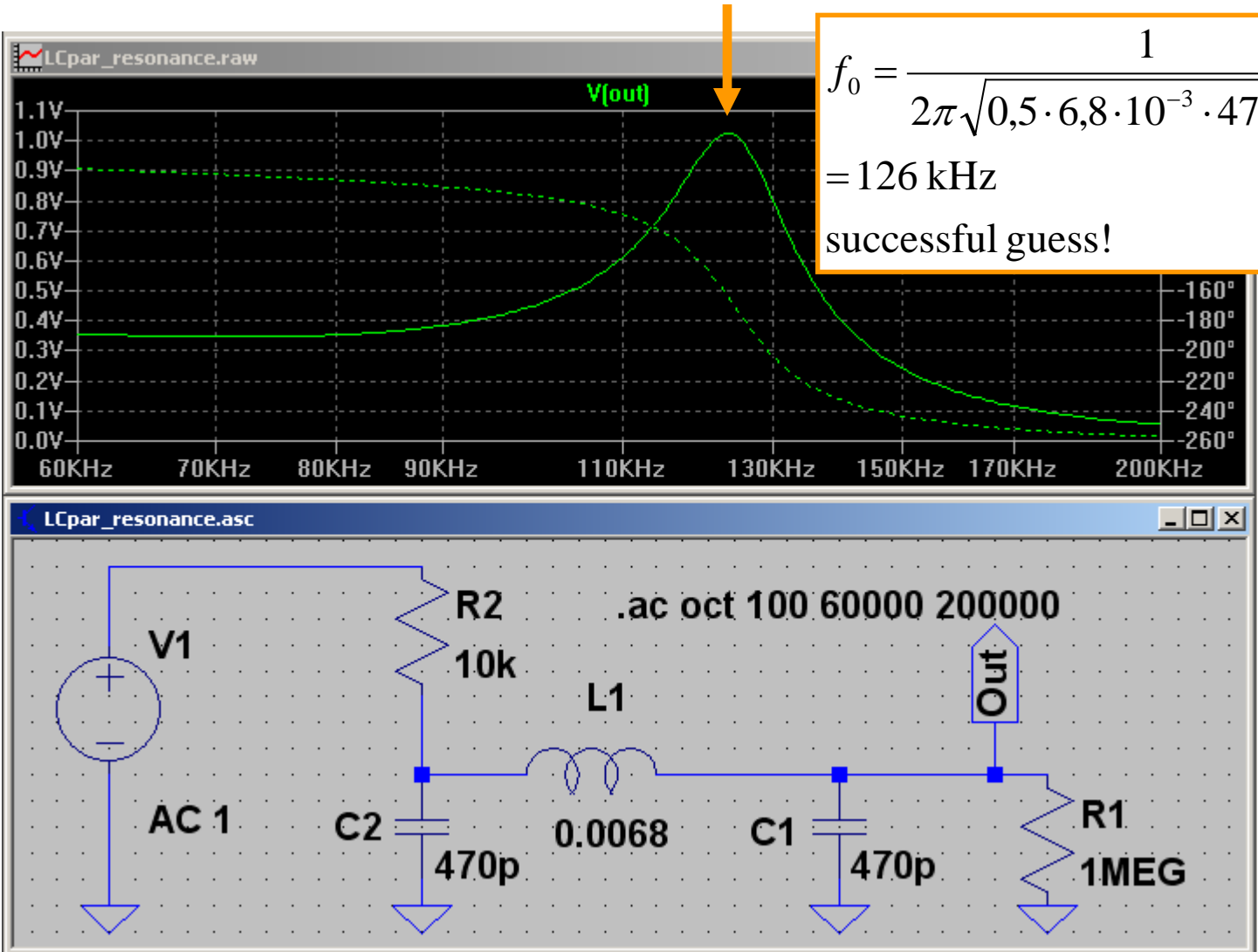
$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C}}$$



The calculations of the circuit is really quite complicated - but we venture to us on a "guess":

$$C_{ERS} = \frac{C \cdot C}{C + C} = \frac{C}{2} \quad f_0 \approx \frac{1}{2\pi\sqrt{L \cdot \frac{C}{2}}}$$



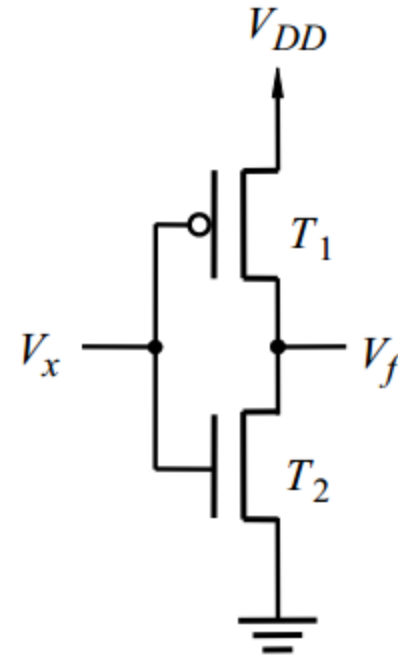
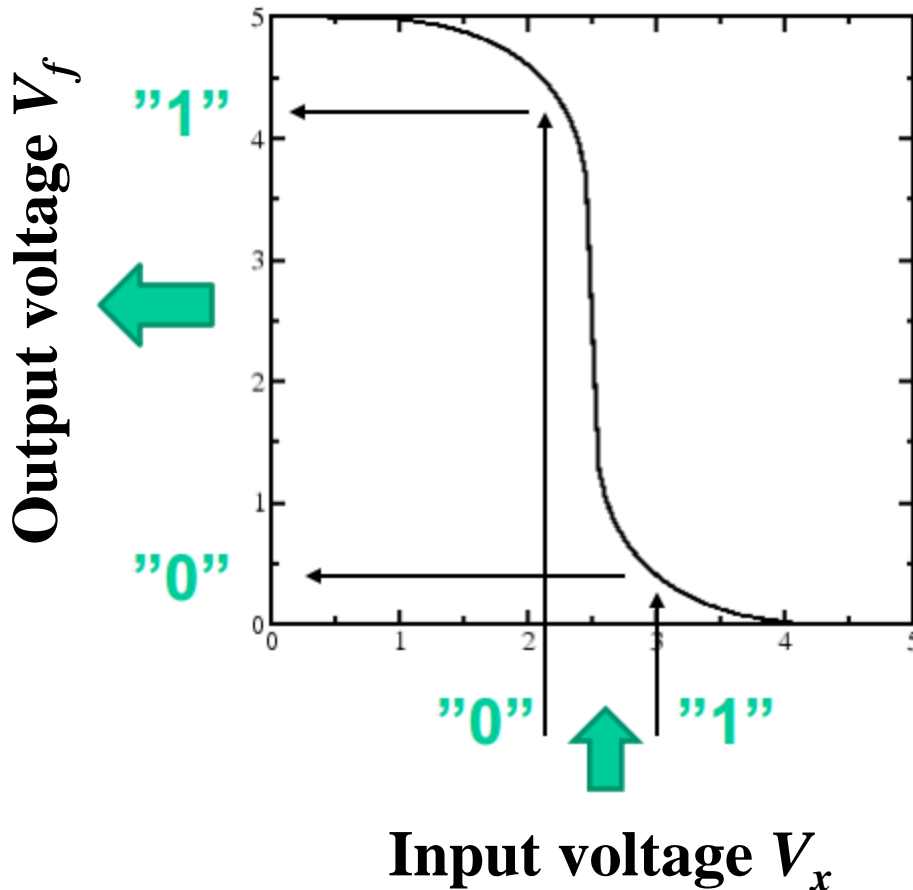


$$f_0 = \frac{1}{2\pi\sqrt{0,5 \cdot 6,8 \cdot 10^{-3} \cdot 470 \cdot 10^{-12}}}$$

= 126 kHz  
successful guess!

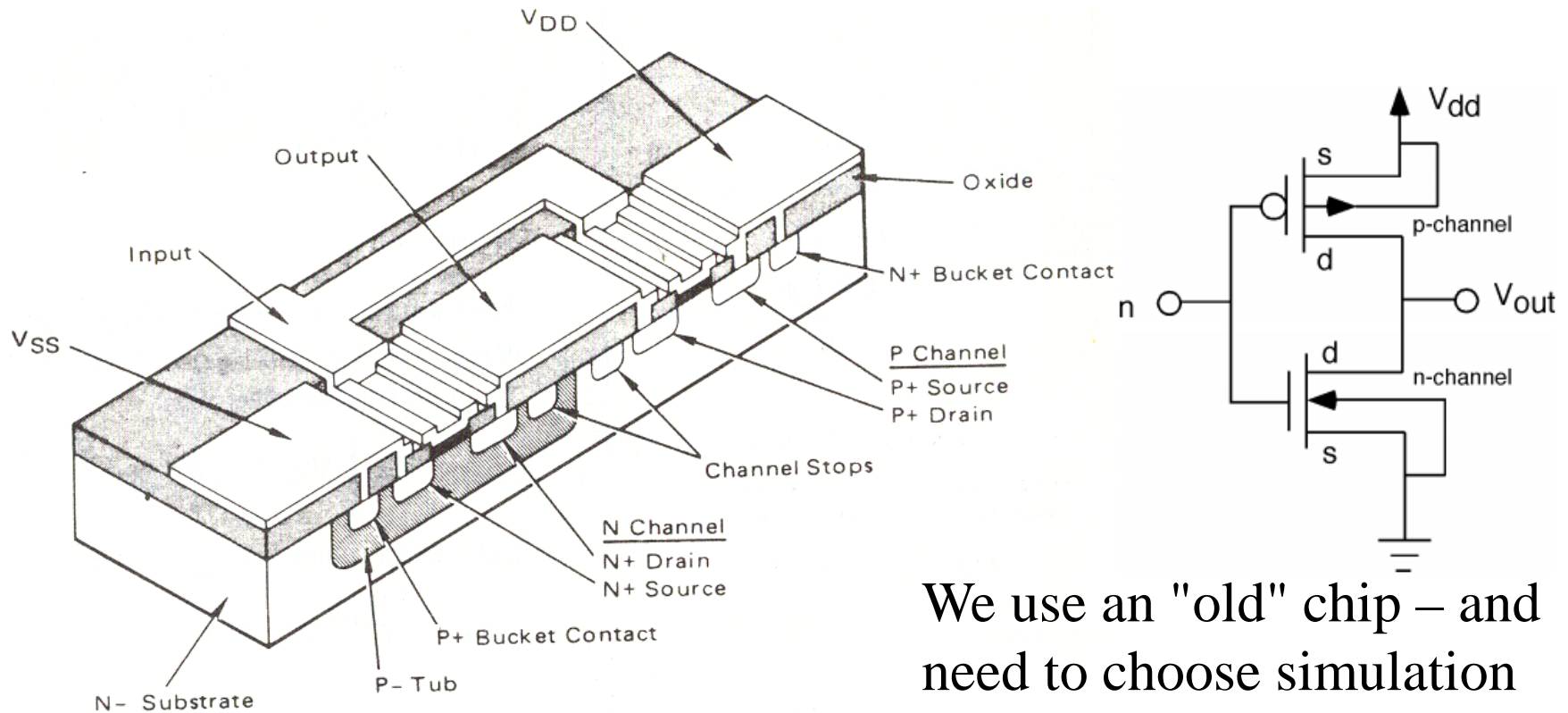
William Sandqvist [william@kth.se](mailto:william@kth.se)

# Digital design – inverter



*Do you remember the CMOS-inverter from Digital Design?*

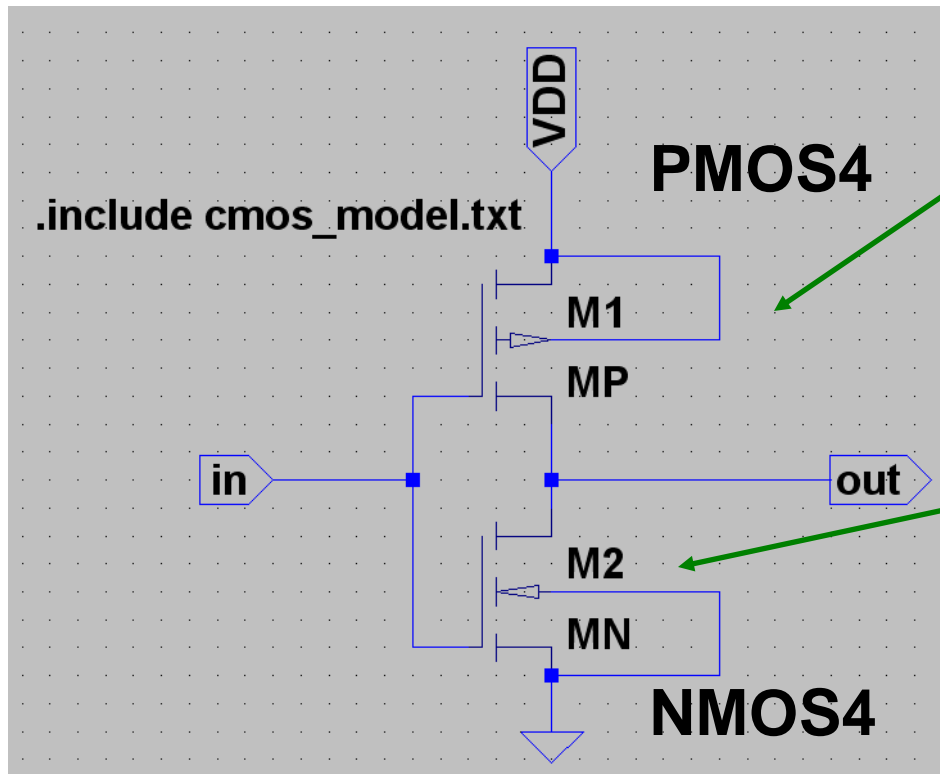
# CMOS-inverter



- *Do you remember the CMOS-inverter from Digital Design??*

We use an "old" chip – and need to choose simulation parameters accordingly!

# ( MOS-Old school )



Monolithic MOSFET - M1

Model Name:	MP	OK
Length(L):	5u	Cancel
Width(w):	480u	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		

MP l=5u w=480u

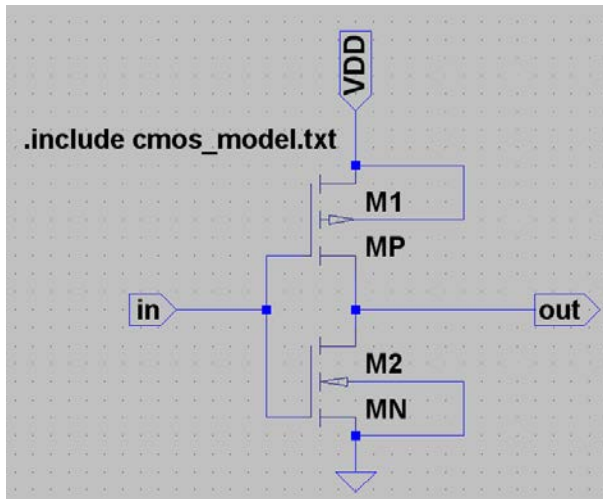
Monolithic MOSFET - M2

Model Name:	MN	OK
Length(L):	5u	Cancel
Width(w):	124u	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		

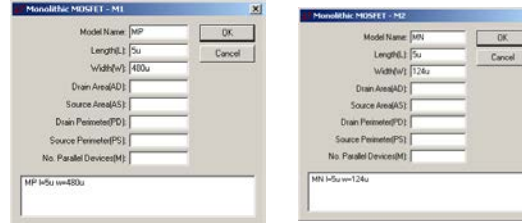
MN l=5u w=124u



# ( MOS-Old school )



Put the file `cmos_model.txt` in your work folder. It contains "scalable" models. Write the directive:  
`.include cmos_model.txt`



## • NMOS

Model Name: **MN**

Length (L): **5u**

Width (W): **124u**

## • PMOS

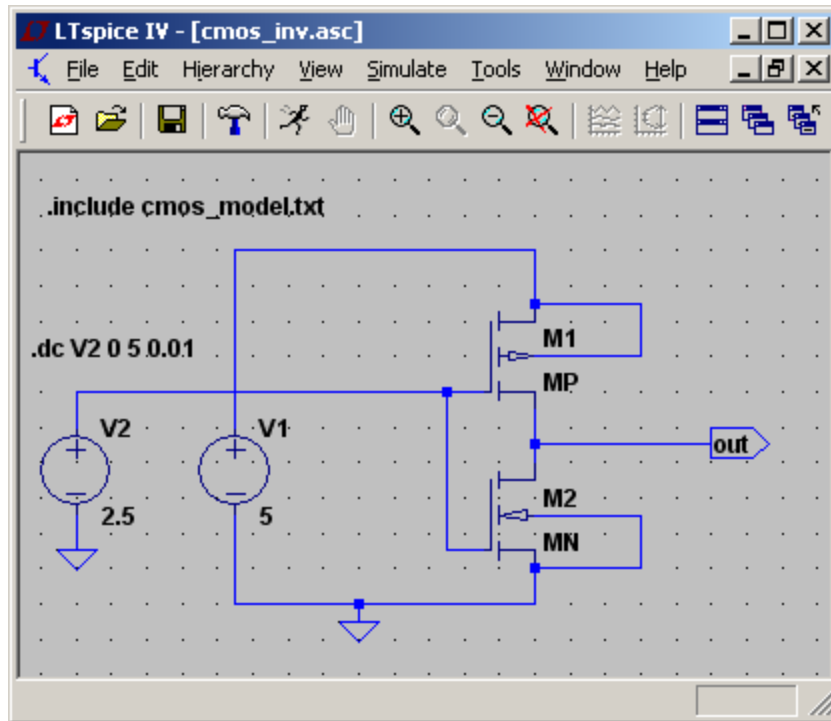
Model Name: **MP**

Length (L): **5u**

Width (W): **480u**

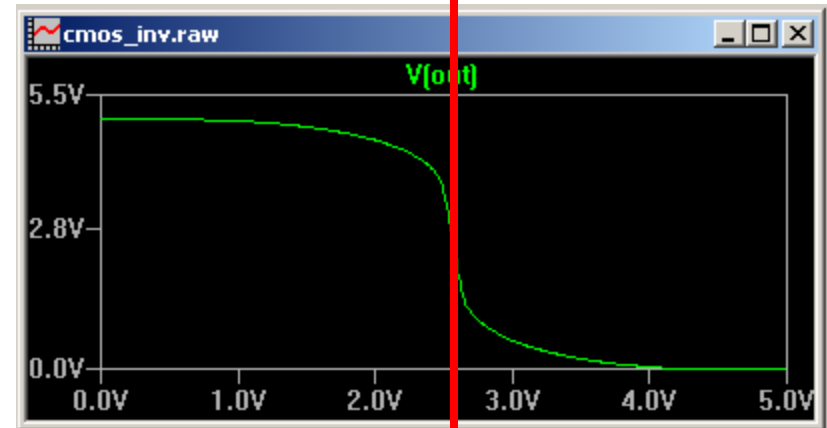
*With these choices  
the two  
transistors will  
get equal  
strength!*

# ( CMOS-inverter)



Simulate with dc- sweep :

```
.dc V2 0 5 0.01
```

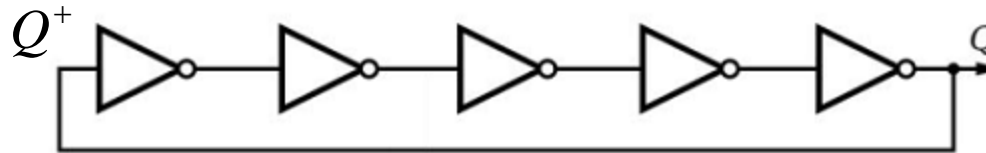
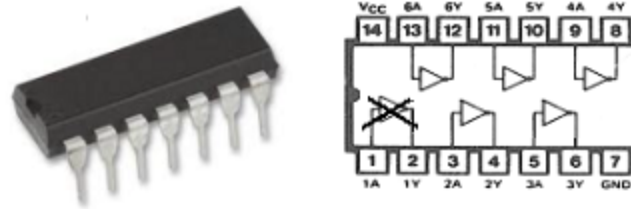


2,5 V

Transistors with equal strength will have the transition at 2,5V.

*Written exam  
in DigDes!*

# Ring-oscillator

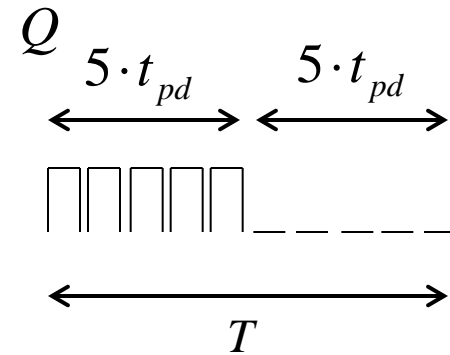
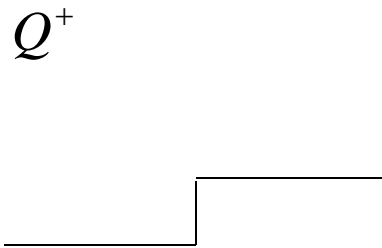


- A ring oscillator consisting of an odd number of inverters connected in feedback.

$$Q^+ = f(Q)$$

$Q$	$Q^+$
0	1
1	0

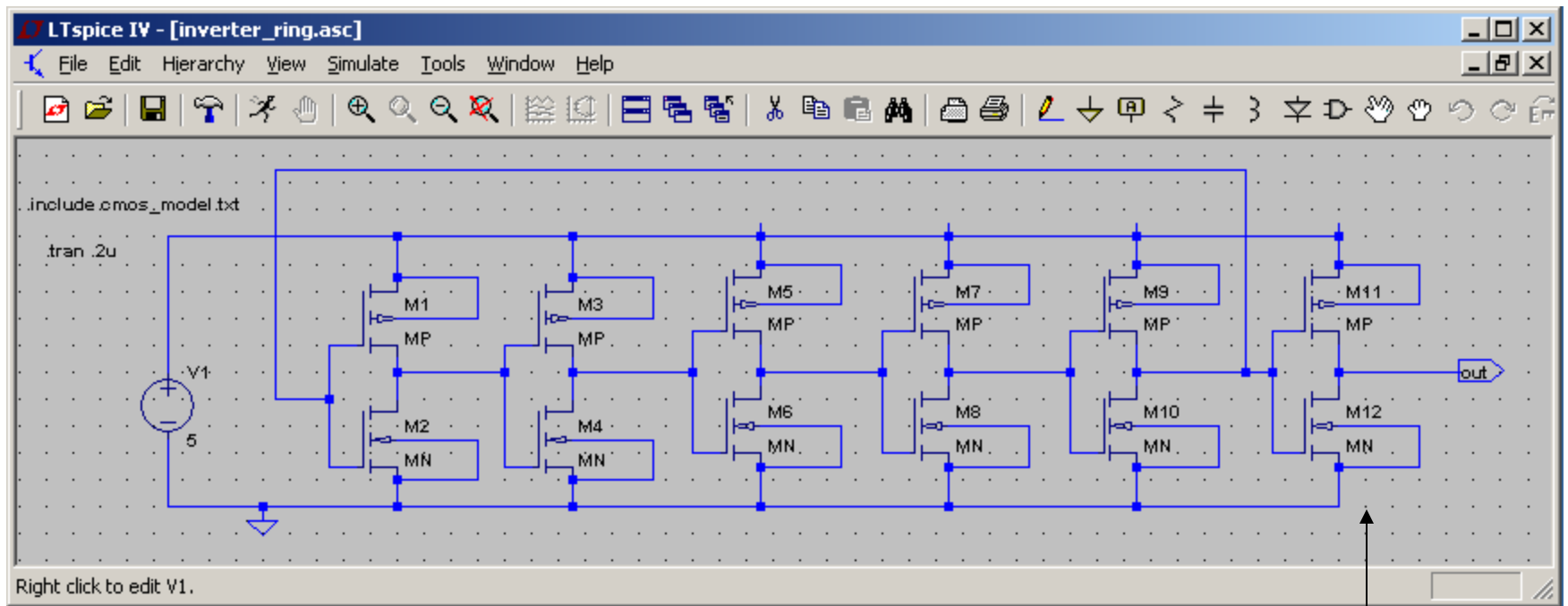
$$T = 2 \cdot 5 \cdot t_{pd} \quad f = \frac{1}{T}$$



# Ring-oscillator



Copy the inverter 5 times! (Vi have a chip with 6 inverters)



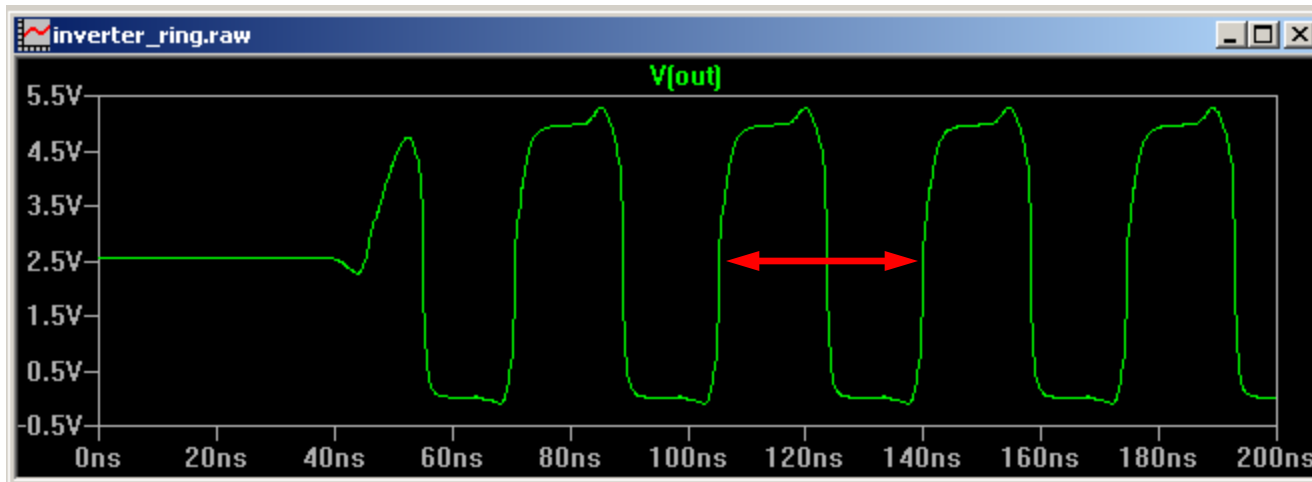
5 inverters in "ring"

+ Buffer

# Ring-oscillator



Simulate with: `.tran .2u`



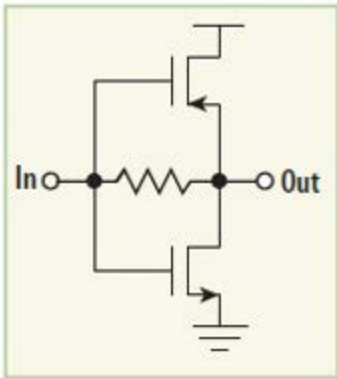
Propagation delay  
of one inverter:

$$t_{PD} = \frac{35}{5+5} = 3,5 \text{ ns}$$

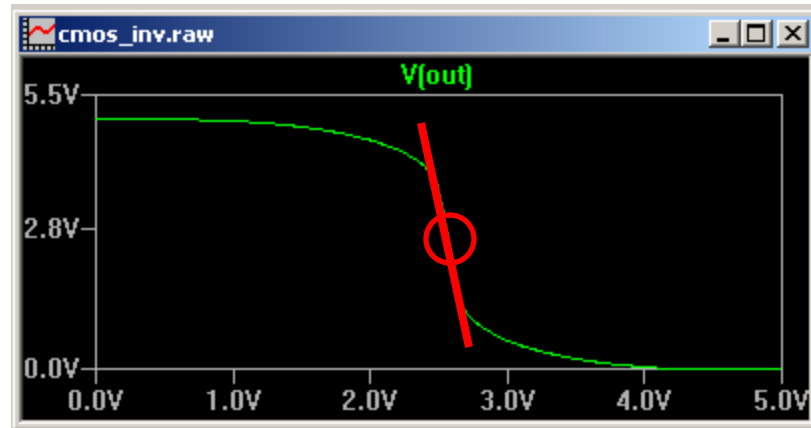
The ring oscillator can be used to indirectly measure the gate delay of the logic circuits!

William Sandqvist [william@kth.se](mailto:william@kth.se)

# Amplifier



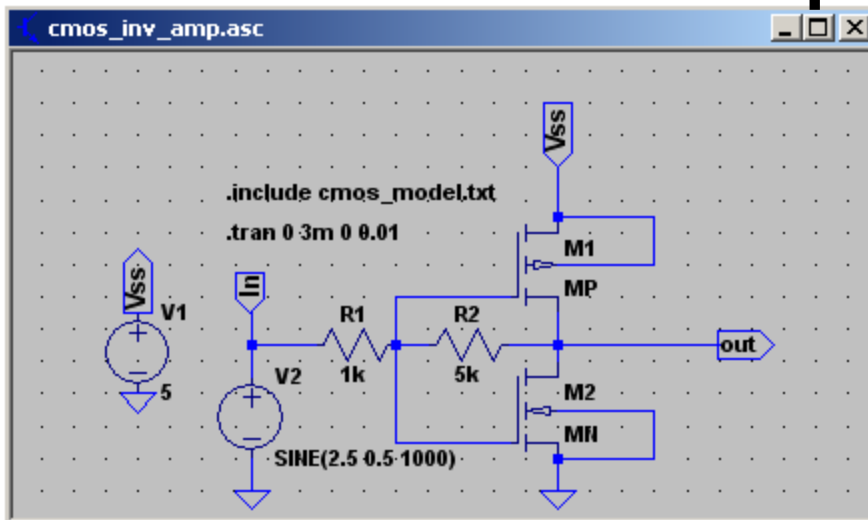
$U_{out}$



$U_{in}$

If feedback the output to the input  $U_{out} = U_{in}$  on a inverter then the voltage will the voltage end up between "1" and "0". The slope is steep, so an input voltage variation is greatly enhanced. A positive input signal shift gives rise to an enhanced negative output voltage change, so we have  $180^\circ$  phase shift.

# Amplifier



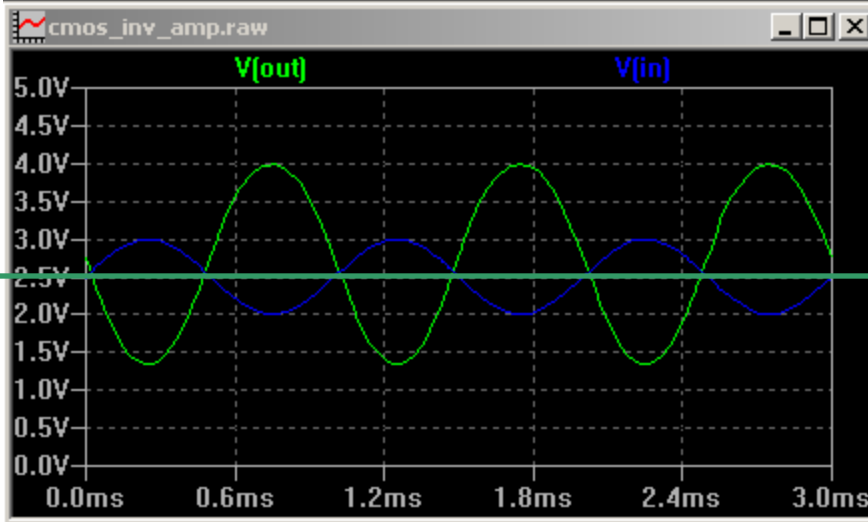
$U_{in}$ : 0,5 V (top value)  
sinusoidal voltage (at the  
2,5V level)

$U_{out}$ : 2,5 V (top value)  
sinusoidal voltage with  
opposite sign **180°** phase  
shift.

Amplification 0,5:2,5    **1:5**

$R1 = 1k$      $R2 = 5k$

(You guessed correctly, the  
amplification is given by  $R2/R1$ )



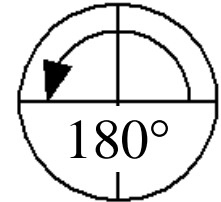


William Sandqvist [william@kth.se](mailto:william@kth.se)

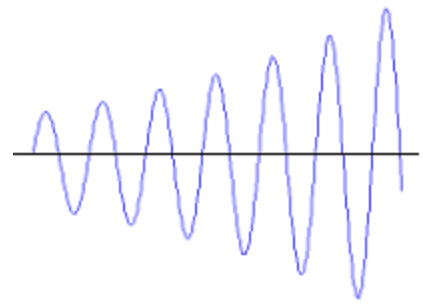
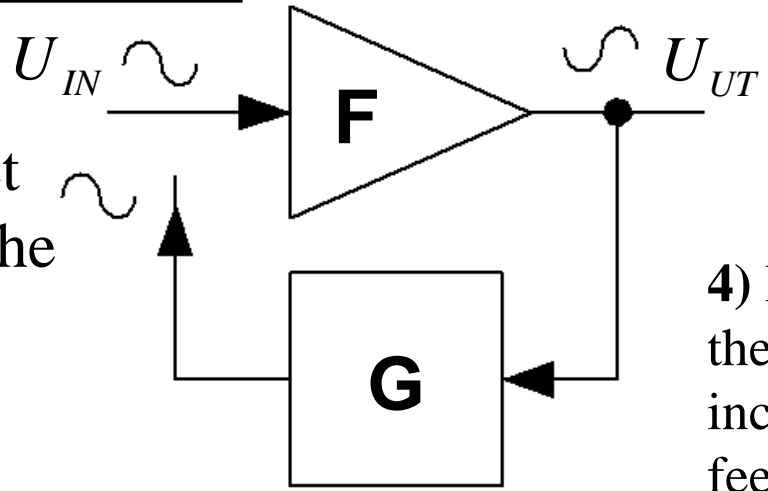
# Can an amplifier become an oscillator?

A feedback amplifier can begin to "oscillate".

1) Amplifier phase shifts signalen  $180^\circ$  (= opposite sign)

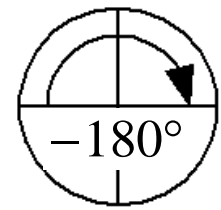


3) Then we get an "copy" of the input signal.



4) If this "copy" is amplified, then the output signal will be increased – for every lap in a feedback loop.

2) If the feedback network phase shifts the signal  $-180^\circ$  for some frequency ...



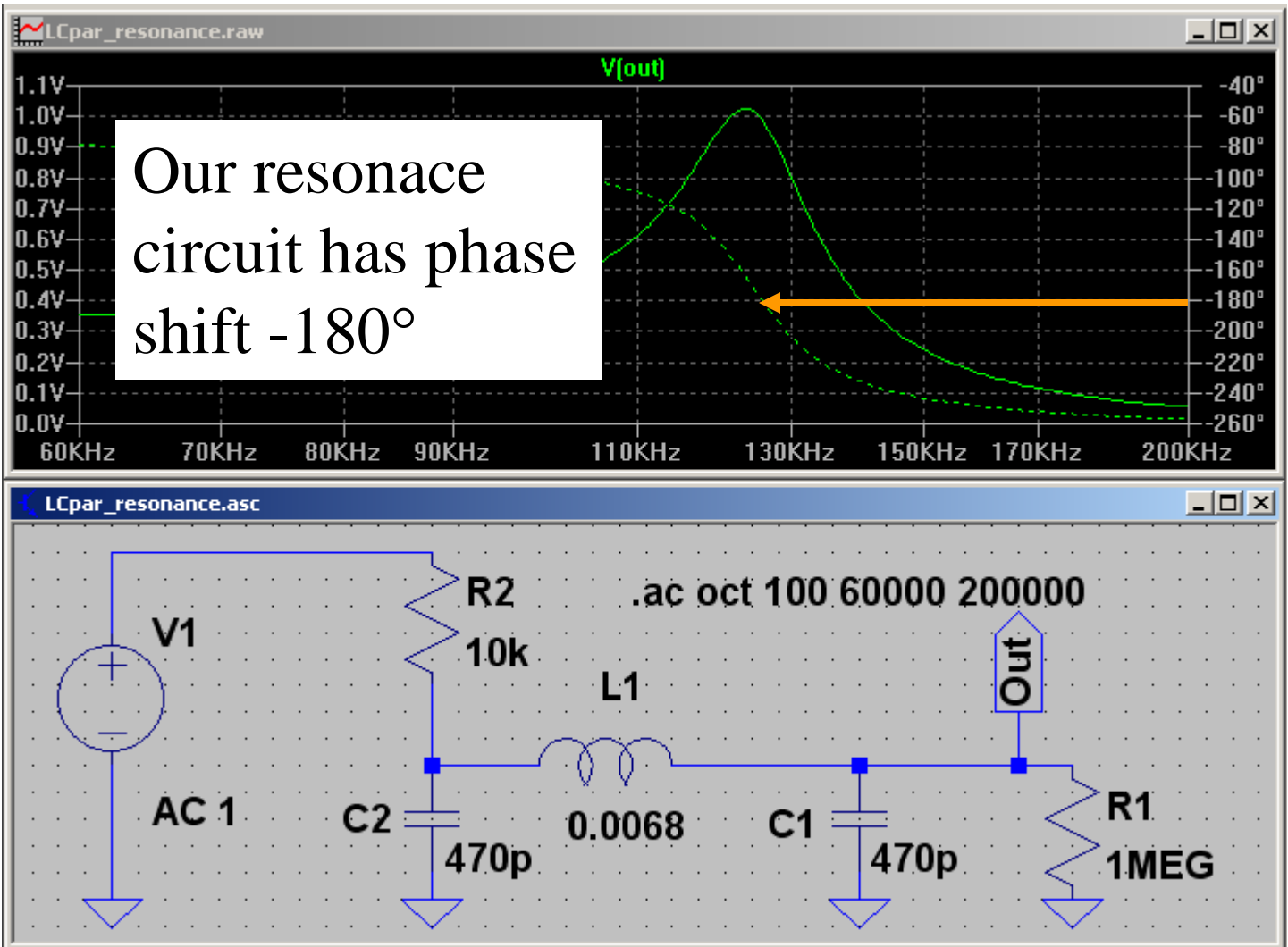
# Can an amplifier become an oscillator?

If the total phase shift in the blocks  $F$  and  $G$  is  $0^\circ$  for some frequency, and at the same time there is a net gain ( $>1$ ) for that frequency – then the amplifier will oscillate with that frequency!

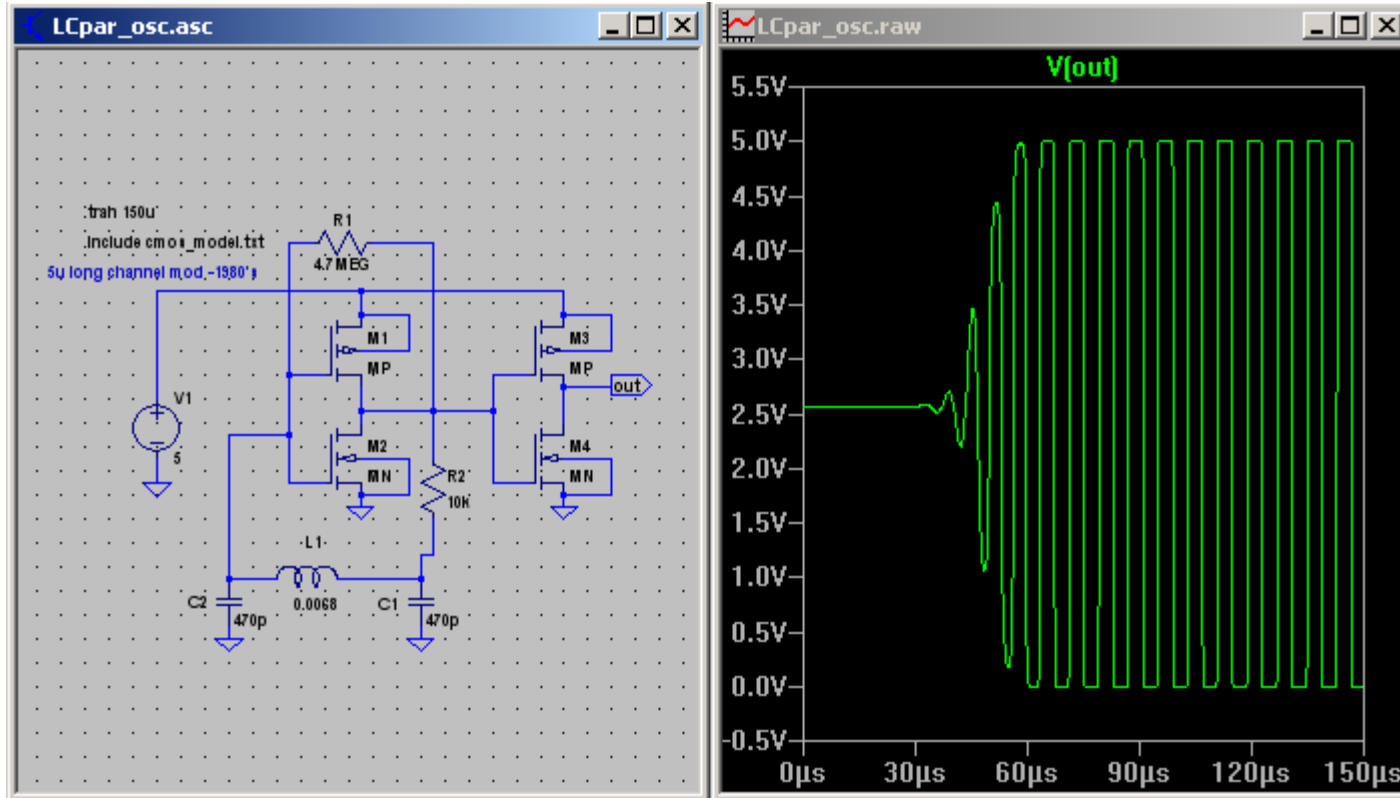


Harry Nyquist

This is known as the Nyquist criterion for stability!

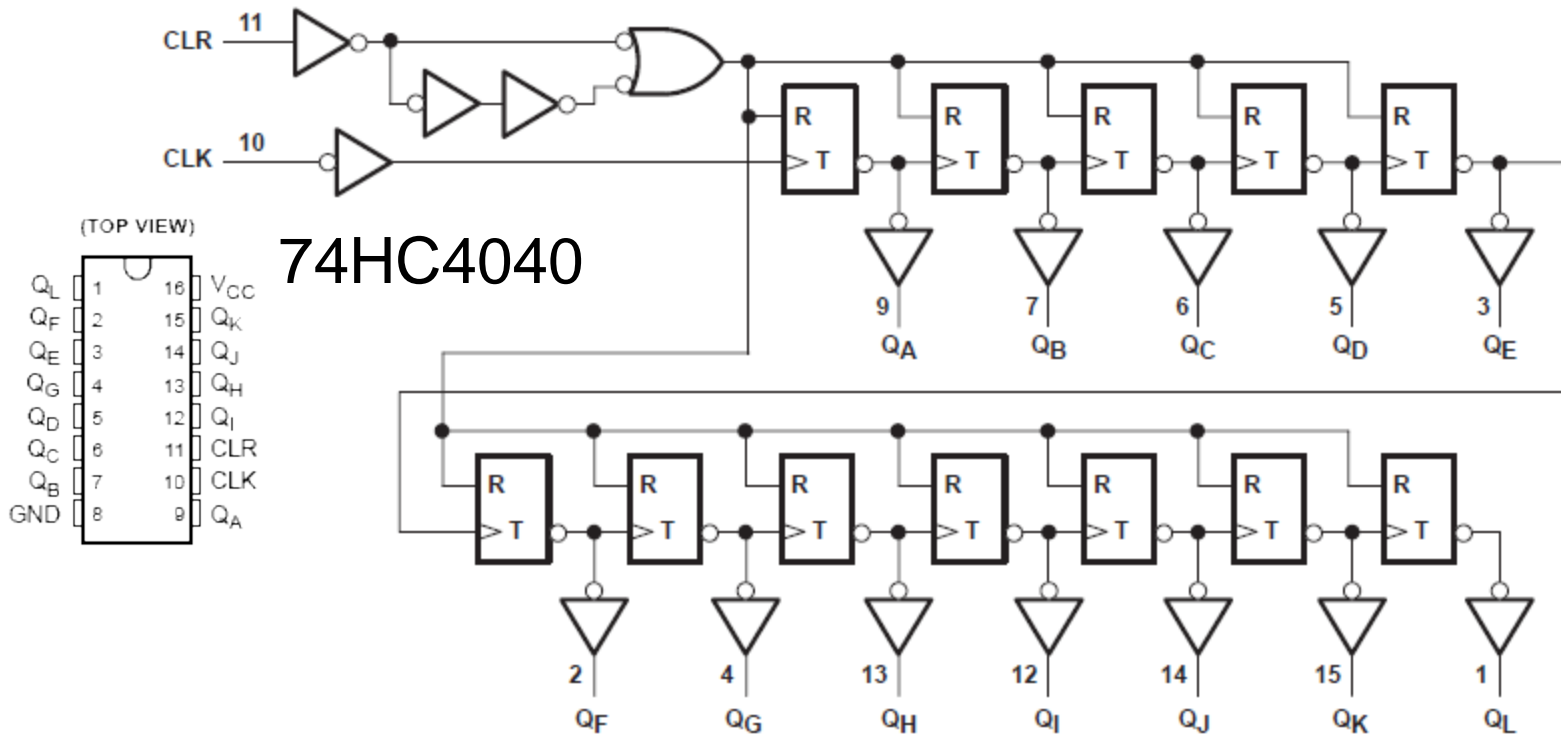


# Oscillator



Oscillator at lab. One inverter has feedback from the resonance filter. One extra inverter acts as a buffer to make the signal digital.

# A counter chip



At lab we use a cheap counter chip. Oscillator frequency is divided with up to 12 stages – to an audible signal. (You've heard about this chip in the Digital Design Course).

William Sandqvist [william@kth.se](mailto:william@kth.se)