



KTH Informations- och kommunikationsteknik

Written exam with solutions for IE1204/5 Digital Design Monday 27/10 2014 9.00-13.00

General Information

Examiner: Ingo Sander.

Teacher: Elena Dubrova /William Sandqvist, tel 08-7904487

Exam text does not have to be returned when you hand in your writing.

Aids: No aids are allowed!

The exam consists of three parts with a total of 12 tasks, and a total of 30 points:

Part A1 (Analysis) contains eight short questions. Right answer will give you one point for six of the questions and one or two points for two of the questions. Incorrect answer will give you zero points. The total number of points in Part A1 is **10 points**. To **pass the Part A1 at least 6p are required, if you get fewer points we will not look at the rest of your exam.**

Part A2 (Methods) contains two methodology problems of a total of 10 points.

To **pass the exam** at least **11 points** from A1 + A2 are required, *if you get fewer points we will not look at the rest of your exam.*

Part B (Design problems) contains two design problems of a total of 10 points.

NOTE ! At the last page of the exam there is a submission sheet for Part A1, which should be separated and submitted together with the solutions for A2 and B.

For a passing grade (E) at **least 11 points required on the exam.**

Grades are given as follows:

0 –	11 –	16 –	19 –	22 –	25
F	E	D	C	B	A

The result is expected to be announced before Monday 17/11 2014.

Part A1: Analysis

Only answers are needed in Part A1. Write the answers on the submission sheet for Part A1, which can be found at the end of the exam text.

1. 1p/0p

A function $f(x, y, z)$ is described by the equation:

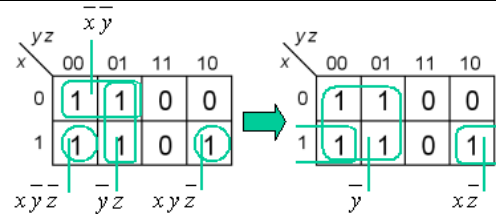
$$f(x, y, z) = \bar{x}\bar{y} + \bar{y}z + x\bar{y}\bar{z} + xy\bar{z}$$

Write the function in a minimal sum-of-products form!

$$f(x, y, z) = \{SoP\}_{\min} = ?$$

1. Solution proposal

$$f(x, y, z) = \bar{x}\bar{y} + \bar{y}z + x\bar{y}\bar{z} + xy\bar{z} = \{Kmap\} = \bar{y} + x\bar{z}$$



2. 2p/1p/0p

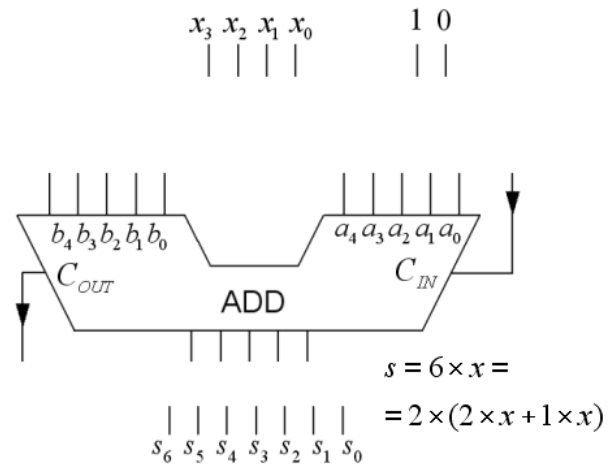
A four bit number $x (x_3x_2x_1x_0)$ is to be multiplied by the constant 6.

The number x is fed into a five bit adder which is configured for the operation $6 \cdot x = 2 \cdot (2 \cdot x + 1 \cdot x)$.

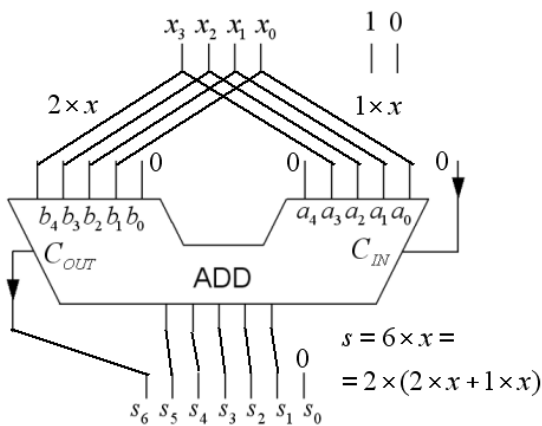
a) Draw how the adder has to be configured. Except the four bits in x , constants with the values 0 and 1 are also available. You will find a copy of the figure on the submission sheet.

b) Which is the greatest binary number $s (s_6s_5s_4s_3s_2s_1s_0)$ that can appear on the output when the circuit is configured for this operation?

Answer with a binary number.



2. Solution proposal a)



b) The greatest number will be $s_{\max} = 6 \cdot 15 = 90$. Since the calculator is not allowed at the exam, this time we can choose to transform 90 to at **binary number** in the same way as in a)

(also other conversion method are ok):

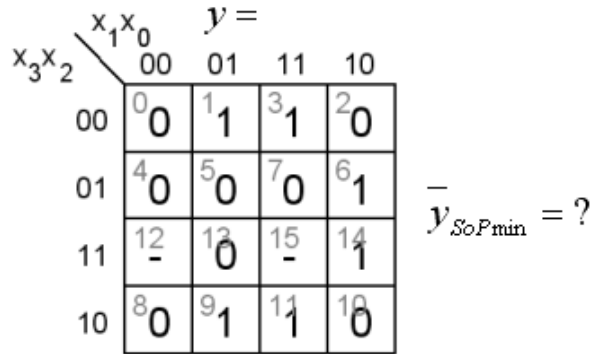
$$\begin{array}{r} \underline{1} \ \underline{1} \ \underline{1} \ \underline{1} \ \underline{0} \ \underline{0} \\ 0 \ \underline{1} \ \underline{1} \ \underline{1} \ \underline{1} \ 0 \quad 15 \times 2 \\ + 0 \ 0 \ \underline{1} \ \underline{1} \ \underline{1} \ \underline{1} \quad 15 \times 1 \\ \hline 1 \ 0 \ 1 \ 1 \ 0 \ 1 \\ 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 0 \quad \times 2 \end{array}$$

3. 1p/0p

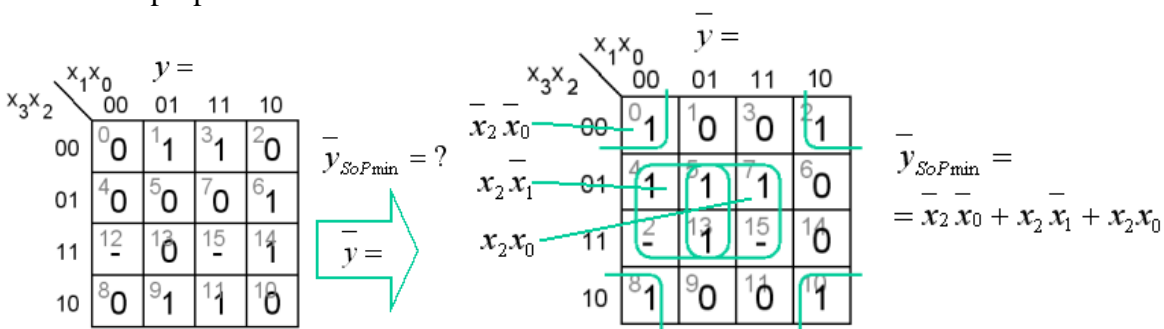
A Karnaugh map for a function of four variables $y = f(x_3, x_2, x_1, x_0)$ is given below.

Write the **inverted function** in a minimal sum of products, SoP, form.

"-" in the map means "don't care". (NOTE that we are asking for the inverse of the function).

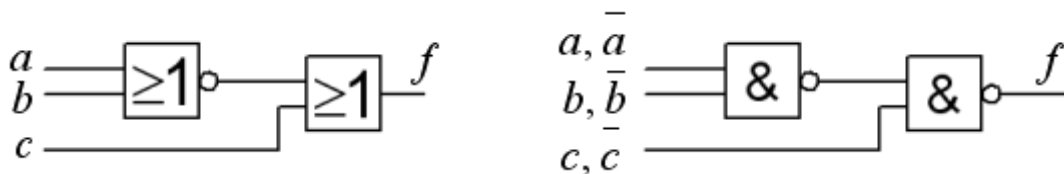


3. Solution proposal



4. 2p/1p/0p

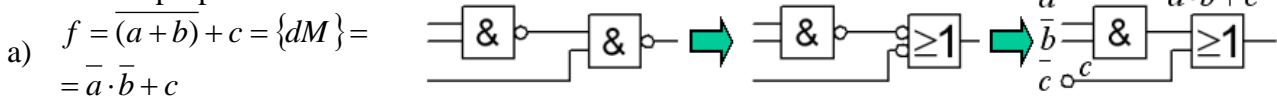
The Figure below shows a kombinatorial circuit consisting of a NOR-gate and an OR-gate (to the left in the figure).



a) Write the logic function $f = f(a,b,c)$ that is realized by the circuit.

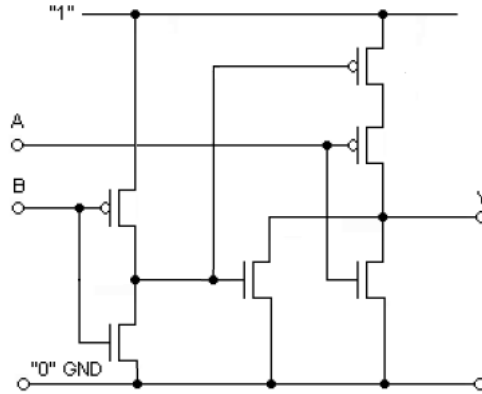
b) The same function can be realized by a NAND-NAND-circuit (to the right in the figure). Write if the variables a, b and c need to be inverted or not at the inputs of this circuits.

4. Solution proposal



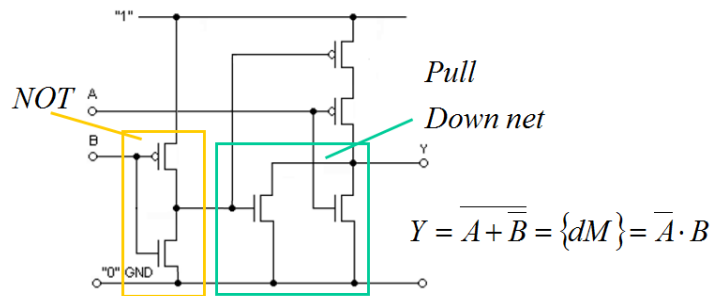
5. 1p/0p

Give an expression for the logical function realized by the CMOS circuit in the figure below?

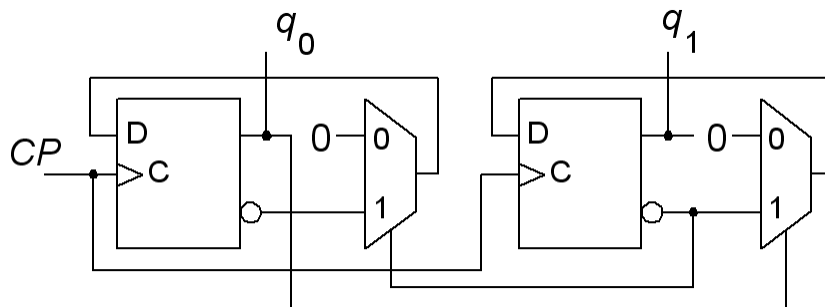


5. Solution proposal

The inverter inverts input signal B. In the Pull Down net the transistors are in parallel. The Pull Down net inverts the function. By using de Morgan's rules the expression can be simplified (not necessary).

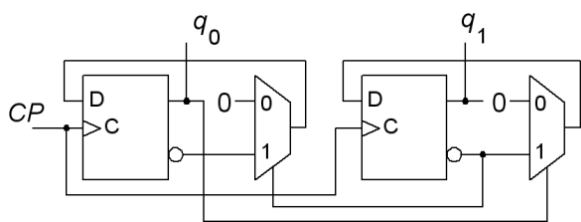


6. 1p/0p



Sequential circuit shown above starts in the state q_1q_0 00. Analyze the circuit and give the sequence of its states for the following four clock pulses.

6. Solution proposal



$$q_1^+ = \bar{q}_1 \cdot 0 + q_0 \cdot \bar{q}_1 = \bar{q}_1 q_0$$

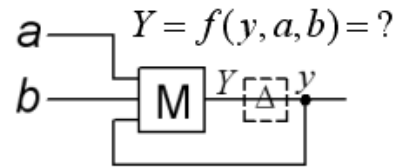
$$q_0^+ = q_1 \cdot 0 + \bar{q}_1 \cdot q_0 = \bar{q}_1 q_0$$

$q_1 q_0$	\rightarrow	$q_1^+ q_0^+$
00	\rightarrow	01
01	\rightarrow	10
10	\rightarrow	00
00	\rightarrow	01

7. 1p/0p

This figure shows an asynchronous sequential circuit. The gate with the letter *M* is a majority gate – which means that the output takes the same value as the majority of its inputs. Analyze the circuit and write its characteristic function.

$Y = f(y, a, b) = ?$



7. Solution proposal

	<i>ab</i>				
<i>y</i>	00	01	11	10	
0	0	0	1	0	$Y = ab + yb + ya$
1	0	1	1	1	

8. 1p/0p

This VHDL-code describes a known circuit. Which one? Choose between:

- a. A half adder.
- b. A full adder.
- c. two XNOR-gates.
- d. A JK-flip-flop.
- e. A SR-latch.
- f. A 2x2 crossbar switch.
- g. A multiplication circuit.
- h. A division circuit.

```

ENTITY gismo IS
PORT ( c, b, a : IN  STD_LOGIC ;
       x, y     : OUT STD_LOGIC ) ;
END gismo ;

ARCHITECTURE beh OF gismo IS
BEGIN
  x <= c XOR b XOR a ;
  y <= (a AND b) OR (c AND a) OR (c AND b) ;
END beh ;

```

8. Solution proposal

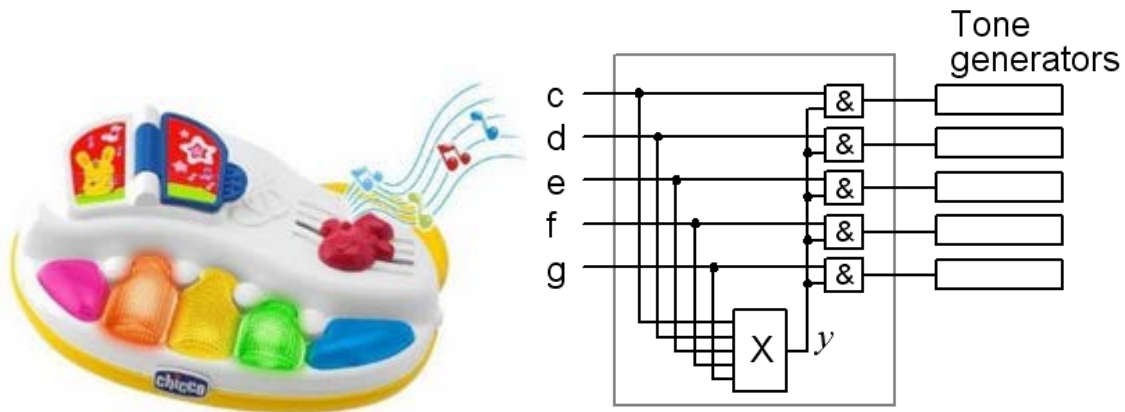
- b. A full adder.

Part A2: Methods

Note! Part A2 will only be corrected if you have passed part A1 ($\geq 6p$).

9. 4p Toy instruments for young children can be very disturbing. You must therefore construct a "dissonance-lock" representing the block **X** in the figure. You should be able to press the keys one at a time, but if you press multiple keys simultaneously, a chord, then just (= the nice sounding) combinations of keys, c, e, and g should sound, other combinations should be quiet.

The sound should be produced only if (1) exactly one of the keys c, d, e, f, g, is pressed (2) any possible combination of keys c, e, g is pressed. All other combinations produce no sound.



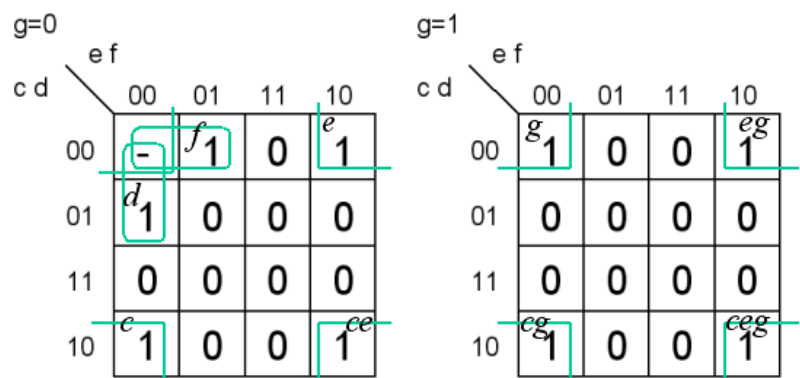
- (1p) Set up the truth table $y = f(c, d, e, f, g)$ or draw a Karnaugh map directly.
Can you find a case where the value of y does not matter? If so, use it as a don't care (it will pay off).
- (1p) Minimize the function y and express it in a sum of products (SoP) form. Use don't cares.
- (1p) Invert the minimized function y from b) with the help of the de Morgan rules.
- (1p) You are restricted to use only four input NOR gates for realizing the function.
(Hint! If one NOR gate is used as an inverter at the output of the circuit, then you can use the inverse function from c).

Thank you for designing this circuit - many parents of young children will thank you!

9. Solution proposal

a) $y = 1$ for c, d, e, f, g, ceg, ce, cg, eg totally there will be nine ones.

If no key is pressed, then we don't need to have $y = 0$, as no sound will be generated, y can as well be $y = 1$, so we can use this case as don't care, $y = -$.

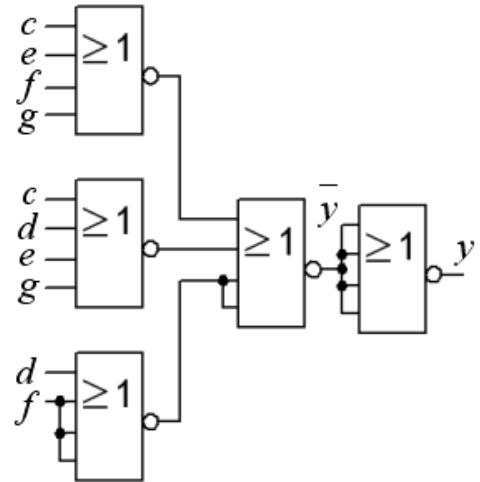


b)

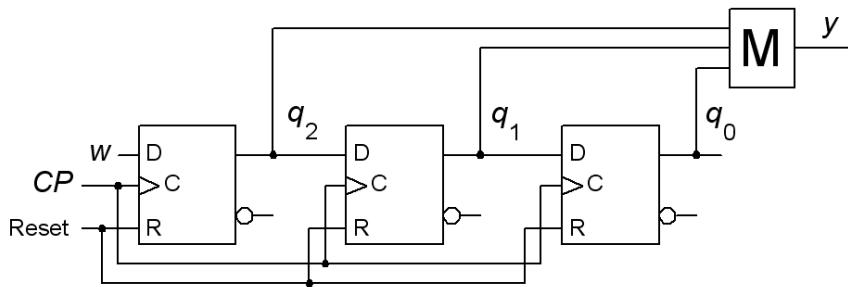
$$y = \overline{c e f g} + \overline{c d e g} + \overline{d f}$$

c)

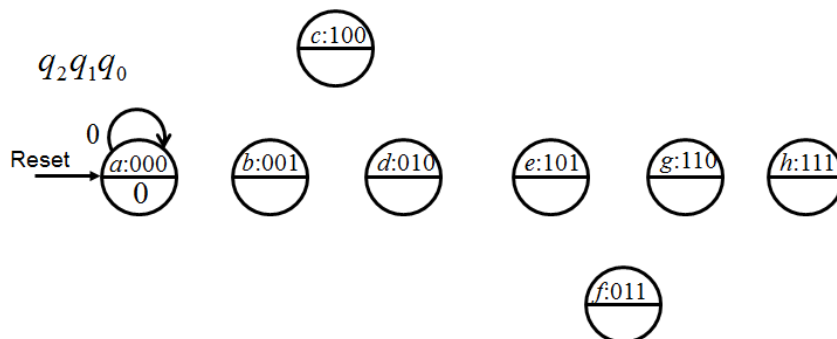
$$\begin{aligned} \overline{y} &= \overline{\overline{c e f g} + \overline{c d e g} + \overline{d f}} = \{dM\} = \overline{(\overline{c e f g}) \cdot (\overline{c d e g}) \cdot (\overline{d f})} = \\ &= (c + e + f + g)(c + d + e + g)(d + f) \end{aligned}$$



10. 6p A synchronous sequential circuit based on a shift register is used as a "Majority voter". The value of the input signal w that occurred most of the times in the past three clock pulses is displayed at the output y . The gate denoted by the "M" is a so-called majority gate, it's output takes the same value as the majority of its inputs.



a) (2p) Analyze the shift register and draw **state diagram** and **state table**. (Please take the help of the initiated state diagram with eight states shown below, but draw your own figure to answer).

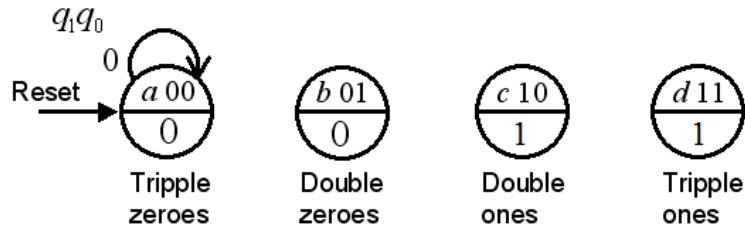


b) (3p) Alternatively, one can make a *similar* circuit in a different way as a Moore machine with four states (not exact the same behavior). Draw the **state diagram** and **state table** for such sequential circuit. Then write the expressions for the **next state** and **output function**. Use the state assignment q_1q_0 00, 01, 10, 11. Working Names of the states could be "Tripple zeroes" "Double zeroes"

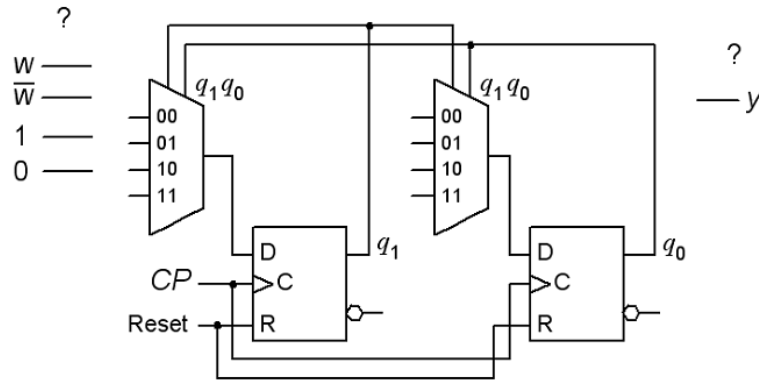
“Double ones” “Tripple ones”.

(Take the help of the figure with the initiated state diagram, but draw your own figure to answer).

$$q_1^+ = f(q_1, q_0, w) \quad q_0^+ = f(q_1, q_0, w) \quad y = f(q_1, q_0)$$

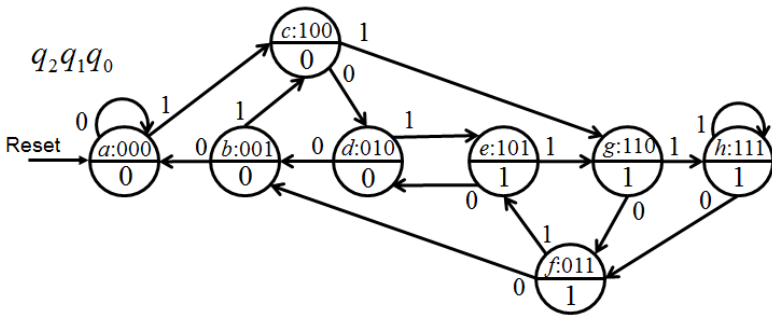


c) (1p) Realize the next state decoder for the circuit in b) with two 4:1 multiplexers. Assume that the signal w is available inverted (if needed). See the figure below, but draw your own figure to answer.



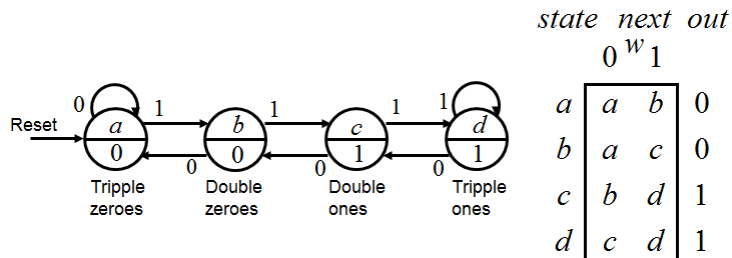
10. Solution proposal

a)



$q_2 q_1 q_0$	$q_2^+ q_1^+ q_0^+$			y	state next out		
	0	w	1		0	w	1
000	000	100	0	a	a	c	0
001	000	100	0	b	a	c	0
010	001	101	0	c	d	g	0
011	001	101	1	d	b	e	0
100	010	110	0	e	d	g	1
101	010	110	1	f	b	e	1
110	011	111	1	g	f	h	1
111	011	111	1	h	f	h	1

b)



	$q_1^+ q_0^+$	w	y	
	$q_1 q_0$	0	0	
a	00	00	01	0
b	01	00	10	0
d	11	10	11	1
c	10	01	11	1

	q_1^+	w	
	$q_1 q_0$	0	1
	00	0	0
	01	0	1
	11	1	1
	10	0	1

	q_0^+	w	
	$q_1 q_0$	0	1
	00	0	1
	01	0	0
	11	0	1
	10	1	1

$$q_1^+ q_0^+ = f(q_1, q_0, w)$$

$$q_1^+ = wq_0 + wq_1 + q_1q_0$$

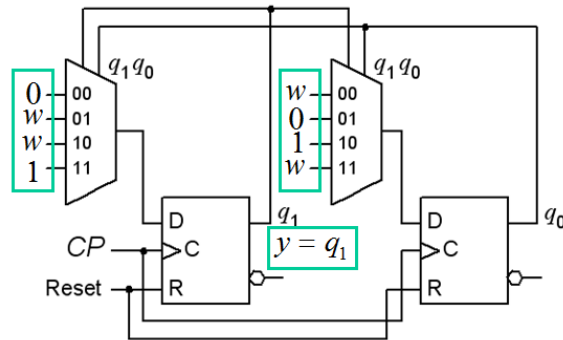
$$y = q_1$$

$$q_0^+ = wq_1 + q_1\bar{q}_0 + w\bar{q}_1$$

c)

	q_1^+	w	
	$q_1 q_0$	0	1
	00	0	0
	01	0	1
	11	1	1
	10	0	1

	q_0^+	w	
	$q_1 q_0$	0	1
	00	0	1
	01	w	0
	11	1	w
	10	w	1



Part B. Design Problems

Note! Part B will only be corrected if you have passed part A1+A2 ($\geq 11p$).

11. 5p Sequence Detector.



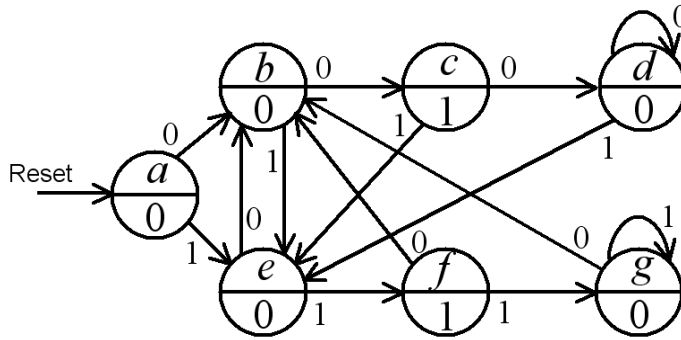
You need to design a synchronous sequential circuit in the form of a positive edge-triggered Moore machine. The input signal w is synchronized with the clock pulses C . The output signal z should become 1 each time the value of the input signal w had not changed for two clock pulses. This change in the output value will appear at the clock pulse following the two pulses with the identical w values. See the example below for clarification.

w: 001100011011100111111000010110 ...
z: 001010100100100101000001000001 ...

a) (3p) Set up the circuit's **state table** and draw the **state diagram**.

b) (2p) Use the binary code to encode the states and set up the **encoded state table**. Obtain the minimized expressions for the **next state** and the **output** functions. No schematic of the circuit needs to be drawn.

11. Solution proposal



state next out

	0	w	1
a	b	e	0
b	c	e	0
c	d	e	1
d	d	e	0
e	b	f	0
f	b	g	1
g	b	g	0

	$q_2^+ q_1^+ q_0^+$	0	w	1	y
a: 000	⁰ 001 ¹ 100	0			0
b: 001	² 010 ³ 100	0			0
c: 010	⁴ 011 ⁵ 100	1			1
d: 011	⁶ 011 ⁷ 100	0			0
e: 100	⁸ 001 ⁹ 101	0			0
f: 101	¹⁰ 001 ¹¹ 110	1			1
g: 110	¹² 001 ¹³ 110	0			0

14 15

$q_2 q_1$	$q_0 w$	q_2^+			
		00	01	11	10
00	0 0	1	3	2	0
01	4 0	5	7	6	0
11	12 0	13	15	-	-
10	8 0	9	11	10	0

$q_2 q_1$	$q_0 w$	q_1^+			
		00	01	11	10
00	0 0	1	3	2	1
01	4 1	5	7	6	1
11	12 0	13	15	-	-
10	8 0	9	11	1	10

$q_2 q_1$	$q_0 w$	q_0^+			
		00	01	11	10
00	0 1	1	3	2	0
01	4 1	5	7	6	1
11	12 1	13	15	-	-
10	8 1	9	11	0	1

$$q_2^+ = w$$

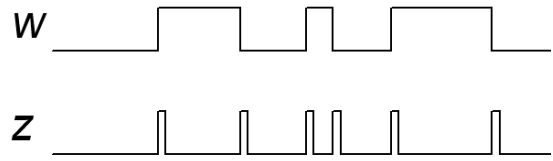
$$q_1^+ = \bar{q}_2 q_0 w + q_2 q_1 \bar{w} + q_2 q_1 w + q_2 q_0 \bar{w}$$

$$q_0^+ = \bar{q}_0 w + q_1 \bar{w} + q_2 \bar{w} + q_2 q_1 q_0$$

$$y = \bar{q}_2 q_1 q_0 + q_2 q_1 q_0$$

12. (5p) Dual edge trigger.

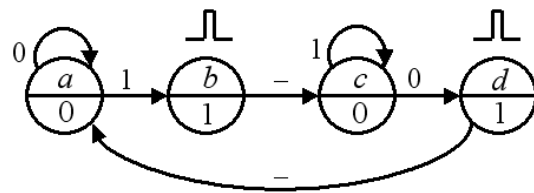
Construct an asynchronous sequential circuit which at each change (0→1 or 1→0) of the input signal w generates a short pulse at the output z . When the input signal is unchanged, the output should be $z = 0$. Output pulse length is given by the time for the transition state in the asynchronous sequential circuit. See timing diagram for clarification.



Your answer must include a **state diagram**, if necessary minimized, a **flow table**, and an appropriate **state assignment** with a **excitation table** that gives race-free networks. You must also develop the hazard-free expressions for the **next state** and an expression for the **output**, and draw the gate circuit. It's free to use any type of gates. Hint: One can intuitively arrive at a solution with four states.

12. Solution proposal

The unstable states b and d with the output signal 1 generates the output pulses. The four states can be encoded by the Graycode 00 01 11 10.



The groupings in the Karnaugh maps are directly free from hazards.

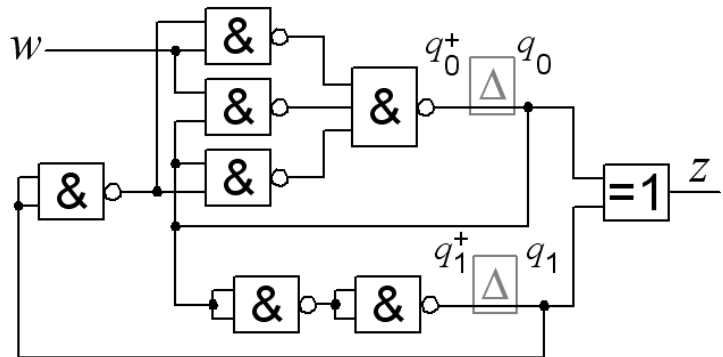
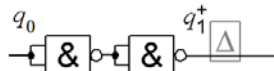
state	next		out	$q_1 q_0$		z	q_1^+		z	q_0^+	
	0	1		0	1		0	1		0	1
a	a	b	0	00	00	01	0	00	0	0	0
b	c	c	1	01	11	11	1	01	1	1	1
c	d	c	0	11	10	11	0	11	1	1	1
d	a	a	1	10	00	00	1	10	0	0	0

$$z = \bar{q}_1 q_0 + q_1 \bar{q}_0 = q_1 \oplus q_0$$

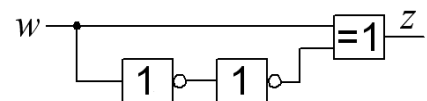
$$q_1^+ = q_0 \quad q_0^+ = w \bar{q}_1 + w q_0 + \bar{q}_1 q_0$$

$$q_0 \quad ? \quad q_1^+ \quad q_1$$

• q_1 "net" consists, according to the expressions, of a "wire", but in order to justify the delay-element we have to insert two inverters – to create the necessary delay!



• An other solution could be to use this combinatorial net which has a glitch at its output, but this would no longer be a sequential circuit.



Submission sheet for Part A1 sheet 1

(remove and hand in together with your answers for part A2 and part B)

Last Name: _____ Given Name: _____

Personal code number: _____

Write down your answers for the questions from Part A1 (1 to 8)

Question	Answer
1	$f(x, y, z) = \{SoP\}_{\min} = ?$
2	<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>a)</p> <div style="text-align: center; margin-bottom: 10px;"> $\begin{array}{cccc} x_3 & x_2 & x_1 & x_0 \\ & & & \end{array}$ </div> <div style="text-align: center; margin-top: 10px;"> $\begin{array}{ccccccc} & & & & & & \\ s_6 & s_5 & s_4 & s_3 & s_2 & s_1 & s_0 \end{array}$ </div> </div> <div style="width: 50%;"> <p>b) $s_{\max} = ?_2$ (answer with a binary number)</p> </div> </div>
3	$\bar{y} = f(x_3, x_2, x_1, x_0) = \{SoP\}_{\min} = ?$
4	<p>a) $f(a, b, c) = ?$</p> <p>b) $a \bar{a}, b \bar{b}, c \bar{c}$</p>
5	$Y = f(A, B) = ?$
6	$q_1 q_0 \ 00,$
7	$Y = f(y, a, b) = ?$
8	a ... h ?

This table is completed by the examiner!!

Part A1	Part A2		Part B		Total	
Points	9	10	11	12	Sum	Grade