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Wafer-level fabrication of individual solid-state nanopores for sensing single DNAs

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Abstract

For biomolecule sensing purposes a solid-state nanopore platform based on silicon has certain advantages as compared to nanopores on other substrates such as graphene, silicon nitride, silicon oxide etc Capitalizing on the developed CMOS technology, nanopores on silicon are scalable without any requirement for additional processing, the devices are low cost and the process can be repeatable with a high yield. One of the essential requirements in biomolecule sensing is the ability of the nanopore to interact with the analyte. In this work, we present a method for processing high aspect ratio, single nanopores in the range of 10–30 nm in diameter and approximately 700 nm in length on a silicon-on-insulator (SOI) wafer. The presented method of manufacturing the high aspect ratio individual nanopores combines optical lithography and anisotropic KOH etching with a final electrochemical etching step to form the nanopores and is repeatable and can be processed in batches. We demonstrate electrical detection of dsDNA translocation, where the characteristic time of the process is in the millisecond range. We also analyse the translocation parameters and correlate the enhanced length of the nanopore to a longer translocation time as compared to other substrates.

Keywords: nanopore, electrochemical etching, DNA, translocation, silicon-on-insulator

(Some figures may appear in colour only in the online journal)

1. Introduction

Solid-state nanopores are considered as a promising candidate for the next-generation platform for a broad range of low-cost, high-throughput molecular diagnostics [1]. The interest in solid-state nanopores has considerably increased since the earliest reported manufacturing of solid-state nanopores [2]. It is widely accepted that nanopores both as a single and as an array can be used for biomolecule sensing experiments. Solid-state nanopores manufactured on silicon nitride [3–5], silicon [6], graphene [7], MoS_2 [8], HfO_2 [9], polyimide [10], PET [11] and others have been demonstrated to detect DNA and proteins at the single-molecule level. By functionalizing the surface of the single solid-state nanopore a similarity towards biological ion channels is demonstrated [12]. One of the drawbacks of these kinds of nanopores has been that they were unable to demonstrate a large scale and repeatable manufacturing process. Solid-state nanopores in silicon provide unique advantages, such as a controlled spacing, potentially low fabrication cost and high yield as compared to the very popular biological nanopore α-Haemolysin. Large scale manufacturing of nanopores that is available at a reasonable cost

may help to accelerate the practical implementation of this detection concept. A low-cost method of fabricating large-scale high aspect ratio individual nanopores with a diameter of ∼2 nm would present a unique platform related to DNA sequencing. But larger nanopores in the range 5–50 nm may also be interesting for other type of applications such as for detection of large proteins, extracellular vesicles (where exosomes have recently attracted a large interest), virus, immune cells etc

There are several methods for the fabrication of nanopores: Shrinking of a large nanopore processed using focused ion beam from approx. 300 nm to a few nm by thermal heating [13], or by electron beam induced heating [14], the formation of a small opening by controlled dielectric breakdown [13, 15], wet etching[16], focused ion beam [17], track-etching [5] and e-beam drilling [18–20] to name a few. Of the several fabrication techniques to fabricate a single nanopore, controlled processing using e-beam lithography on silicon is a well-known method [21, 22]. However, due to the high equipment cost and low throughput, these methods are expensive and become slow for processing large quantities. With several control parameters that are required to process the nanopores, it is often difficult to repeat the process. In addition, for a measured translocation speed of DNA through a nanopore typically at ∼40 bases μs^{-1} it requires a measurement instrument with high bandwidth [22, 23]. The electrical noise from the nanopore poses serious limitations in identifying different bases. Therefore, a viable solution that meets both low costs in terms of technology and low bandwidth (slow DNA translocation) would ideally contribute significantly towards the efficient detection of DNA and proteins of interest. For the DNA to be detected base by base, there needs to be a technological shift that would help in increasing the time during which the DNA stays in the nanopore. One possibility is by increasing the length of the nanopore which means that slowing the translocation so that the time that each base occupies the nanopore detector preferably is $\geqslant$1 msec [24]. The drawback for long nanopores is that single base pair resolution cannot be achieved using the blocking current and one has to resort to some kind of lateral electrodes.

In this work, we present a wafer-level fabrication method of single or arrays of nanopores using a silicon-on-insulator (SOI) wafer and with such chips, we successfully demonstrate electrical detection of 1000 bp double-stranded (ds) DNA with a long translocation time. The controlled nanopore processing is achieved by an optical lithography step, allowing arbitrary positioning of the nanopores on the surface of a 2 μm thick silicon device layer followed by breakdown electrochemical etching, resulting in high aspect ratio ∼10–30 nm diameter nanopores. Prior work from our group on a similar method has been presented elsewhere [22, 25, 26]. In that case, however, arrays of nanopores were fabricated and detection of translocation was by optical readout using fluorophores. The nanopore diameters, as observed in the SEM images, can be controlled by varying the voltage bias profile of the electrochemical etching. This method of processing a nanopore is fast (∼8 mins), requires fewer control parameters and can be processed on a large scale. For our process, we produced twelve wafers in four batches with 26 devices per wafer in total. The devices were 15 mm × 15 mm in dimension and contained single nanopores as well as array of nanopores. The wafer level fabrication of SOI wafer yielded about 60%–70% with the diameter in the range of 10 nm to 50 nm. Also, we present the electrical measurement of double-strand DNA translocation through a single nanopore. Using electrical methods DNA translocation with these high aspect ratio nanopores has been investigated. A long nanopore allows DNA to be in the nanopore for approx. 1 ms and measures a blockade current of about 680 pA. A low-cost method of fabricating a large-scale high aspect ratio nanopore down to approximately 10 nm presents a unique opportunity in understanding the function and properties of biomolecules.

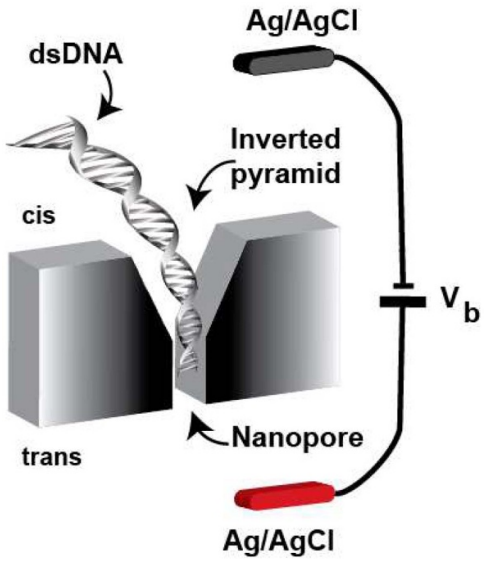

Figure 1. A schematic illustration showing the cross-section of the single nanopore platform with the inverted pyramid for the translocation of dsDNA through the nanopore. The bias voltage V_b is applied across the nanopore to enable the DNA to translocate through the nanopore.

A schematic illustration in figure 1 shows our single nanopore platform with an inverted pyramid on a device layer of an SOI wafer. The main objective is that when a bias is applied across the pore the dsDNA translocates through the nanopore by electrophoresis thus allowing the detection of single DNA translocation events.

2. Materials and methods

In this section, we describe a method used for the fabrication of single solid-state nanopore on a silicon-on-insulator (SOI) wafer. A detailed explanation of the process flow using UV lithography and the electrochemical etching for nanopore processing is presented.

2.1. Single nanopore chip processing

Several approaches can be followed in developing a suspended device layer membrane. The following described process has a lower level of contamination and increases the yield of devices

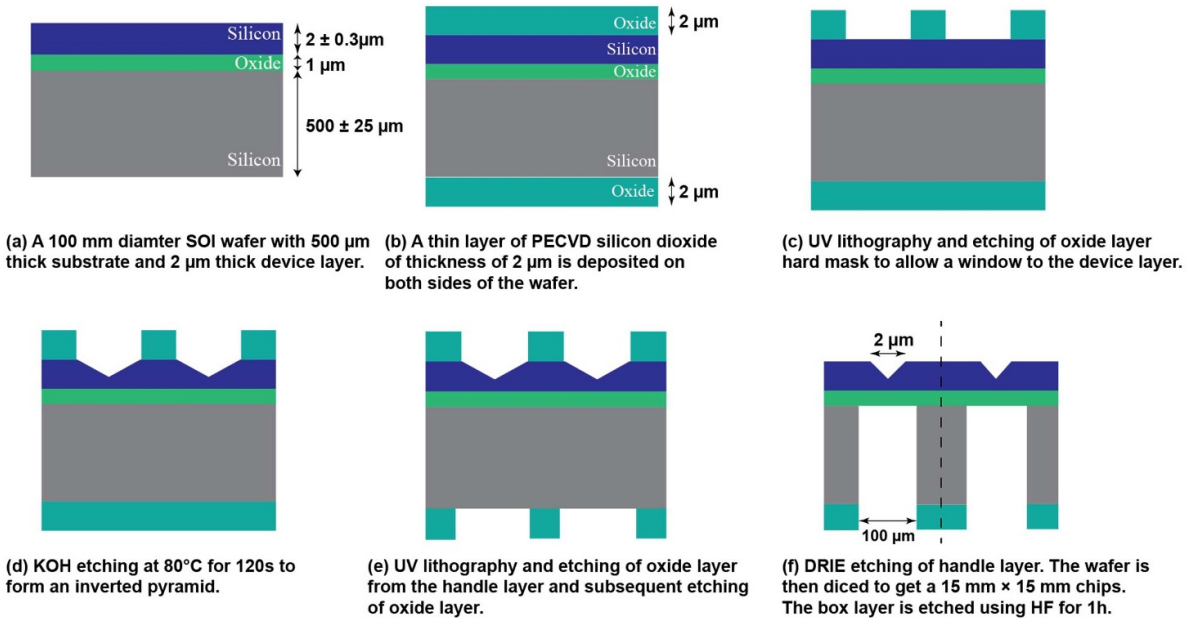

Figure 2. Process flow for producing templates for single nanopore on an SOI wafer. (a) The SOI wafer used contains a device layer of 2 μm thickness with the resistivity in the range of 1–3 Ohm cm. The oxide layer is 1 μm thick and the substrate is approx. 500 μm thick. (b) The deposited PECVD SiO_2 of 2 μm is used as a hard mask (c) The oxide is patterned using UV lithography step and subsequently etched to create 2 μm square openings. (d) KOH etching to achieve inverted pyramidal structures in the device layer. (e) The oxide on the handle layer is patterned using UV lithography and subsequently etched to achieve a 100 µm square window patterning (f) Two-step DRIE etching of the handle layer. The wafer is then diced to get 15 mm × 15 mm chips. The box layer is etched using an HF at the rate of 20 nm min^{-1} for1 h.

when the fabrication is started from the device layer and then followed by ICP etching of the handle layer.

For the nanopore processing, SOI wafers of 500 ± 25 μm thick handle layer and a 2 ± 0.3 μm thick silicon device layer are used with a 1 μm silicon dioxide buried layer. The device layer is chosen to be an n-type with <100> orientation with a resistivity in the range of 1 to 3 Ohm-cm. The process flow is shown in figure 2. The wafer is cleaned with piranha solution with a mixture ratio of (3:1) of (H_2SO_4: H_2O_2), sulphuric acid and hydrogen peroxide for 5 mins and then in 'IMEC-clean', a diluted HF solution, for 120 s. The HF clean removes the native oxide that is present at the surface. This step is followed by a 'standard clean-2', or 'RCA-2 clean' typically at 80 °C for 10 min. This consists of a mixture of (6:1:1) of (H_2O: HCL: H_2O_2). These steps ensure the wafer becomes clean from organic and metal contaminants.

A 2 μm thick layer of PECVD oxide (Plasmalab 80Plus, Oxford systems) is deposited on both sides of the wafer as shown in figure 2(b). The oxide layer serves as a hard mask for further processing of the device and handle wafers. The wafer is subjected to Hexamethyldisilane (HMDS) vapours for a few minutes. This process allows for better adhesion of the photoresist (PR) onto the silicon dioxide surface. For opening a square window to the device layer, a photoresist (SPR 700) layer is spin-coated on the oxide layer with a thickness of 1 μm. The PR is patterned using UV Stepper lithography (Nikon NSR TFHi12) to achieve an array of 2 μm × 2 μm square windows. After exposure, the wafer is heated at 90 °C for 1 min for a post-exposure bake (PEB). During the PEB, the UV exposed region becomes soluble in the developer. The wafer is developed with CD-26 developer for 3 min. The exposed oxide layer is etched using an RIE etcher (Applied Materials Precision 5000 Mark II) for 12 min as shown in figure 2(c). Following the oxide etch, the SOI wafer is dipped in a 30% KOH solution at 80 °C for 120 s. This allows for the formation of an entrance port that has an inverted pyramid shape in the device layer as shown in figure 4(a). This step is critical to achieving a pointed tip at the inverted pyramid shape serving as an initiation point for the following electrochemical etching step. The wafer is rinsed and dried. To protect the device layer from further unwanted processing, a thick layer of 3 μm photoresist is coated on the surface. The wafer is hard baked at 90 °C for 20 min in the oven.

For the handle layer processing (backside), the wafer is coated with an adhesion layer (HMDS) for a few minutes at 150 °C and then spin-coated with a 1 μm thick photoresist (SPR-700). The handle layer pattern on the mask is aligned with the device layer inverted pyramid using a UV Mask aligner (MA6/BA6, Karl Suss) as shown in the schematic figure 2(e). After exposure, the wafer is heated at 90 °C for 1 min for a post-exposure bake (PEB). The wafer is developed with CD-26 developer for 3 min. As a result, a square pattern of size 100 × 100 μm is opened on the photoresist from the backside. The exposed oxide mask is etched with RIE etcher using STS ICP Multiplex Advanced Oxide Etch system for about10 min. Following this step, a deep reactive ion etching (DRIE) of the handle silicon is carried out using STS ICP DRIE as shown in the schematic figure 2(f). The DRIE-Bosch procedure is carried out in two steps. In the first step, the etching is carried out at 13.56 MHz at 15 W power for 150 min at

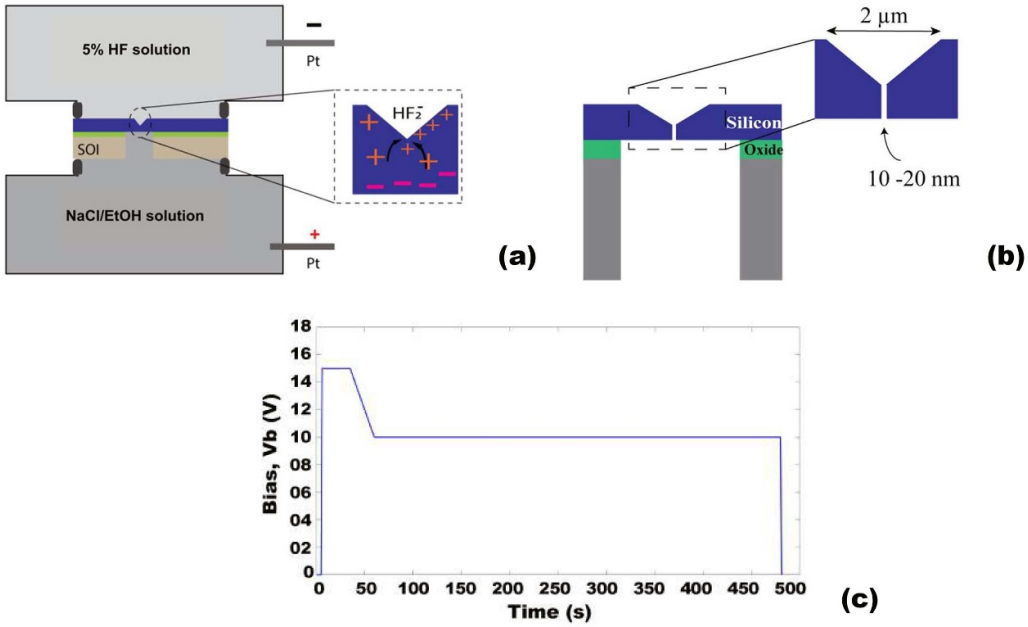

Figure 3. Schematic of the electrochemical etching set-up and the voltage bias profile applied during etching of the nanopore. (a) A Teflon cell with two chambers is used, each equipped with platinum electrodes for electrochemical etching. The set-up shows two chambers that are controlled by a voltage with the chip placed in between. Two O- rings contact on the two faces of the chip to avoid leakage. The upper chamber contains 5% HF and contact to the front side of the chip, while the other chamber contains a salt solution to which a positive potential is applied. The applied bias is generated from a variable DC voltage source. (b) Schematic cross-section of the SOI chip. The inset shows the schematic of a high aspect ratio nanopore obtained after electrochemical etching. (c) The schematic of voltage bias -time duration profile during electrochemical etching. The two-step etching incorporates two different voltages (15 V and 10 V) during etching for a duration of approx. 8 min.

3 μm min^{-1} etch rate, which etches 450 μm of silicon from the handle layer side. The second step is to etch at a low frequency at 380 kHz to minimize notching with a low etch rate at 1 μm min^{-1} for 50 min. This method protects the device layer and buried oxide layers and avoids harm with the aggressive etching by ICP. The result is shown in the SEM image of figure 4(b). Following this, the wafer is diced into small pieces to obtain 15 $\times$ 15 mm chips, each containing a template for single nanopore etching.

2.2. Electrochemical etching of nanopores

Further processing is carried out on the chip level to obtain a long and straight nanopore by electrochemical etching in the breakdown mode. A schematic of the electrochemical etching set-up is shown in figure 3(a). The 1 μm thick BOX layer is removed using diluted HF at a rate of 20 nm min^{-1}. The chip is mounted on a home-built PTFE cell that is filled with 5% HF: H_2O: C_2H_5OH (1:8:3) solution on the device side of the chip and NaCl solution (9 mg ml^{-1}) on the handle layer of the chip. Two O-rings contact on two faces of the chip to avoid liquid leakage. A voltage bias is applied between these two chambers using platinum electrodes which, is inert to the aggressive electrolyte. When a bias (V_b) is applied between the electrodes in the electrochemical cell, the bottom tip of the inverted pyramid experiences a stronger field strength due to the decreased membrane thickness and the high curvature at that point. With sufficient bias, the breakdown field strength can be selectively reached (3 $\times$ 10^5 V cm^{-1}) at the bottom tip of the inverted pyramid as compared to a planar surface. Holes are generated in the breakdown process, thereby initiating electrochemical etching of silicon at pre-defined locations. In addition, the anisotropy of the etching rate plays an important role in the formation of straight pores. At the tip, since the current density equals to the critical current density due to the assumption that a tetravalent reaction happens [27, 28], the current density is the highest along <100> directions of the silicon crystal thus the pores tend to grow along the [001] direction. Figure 3(b) shows a schematic of a long nanopore in the device layer of the silicon chip.

The voltage bias versus time duration that was applied to create a nanopore is shown in figure 3(c). The applied bias is generated from a DC voltage source. Two relays are used to control and switch on and off the circuit to adjust the bias voltage. An optimized voltage bias-time duration profile is required to achieve the desired nanopore diameter. A longer etching time leads to wider diameter of nanopore. A thorough investigation of the relation between the nanopore diameter and the rate of electrochemical breakdown etching is described elsewhere [29]. Each bias profile has two regions: a high bias and a low bias. To initiate the etching at the tip of the inverted pyramid, a high voltage (15 V) is applied for 30 s to trigger avalanche breakdown at the tip, generating holes which are necessary for the electrochemical etching of silicon. The voltage is then lowered gradually for 30 s to 10 V and held stable for 7 mins to continue etching perpendicular to the device layer in the breakdown regime [27]. To minimize the pore diameter and to ensure smooth sidewalls of the pore, the voltage bias is

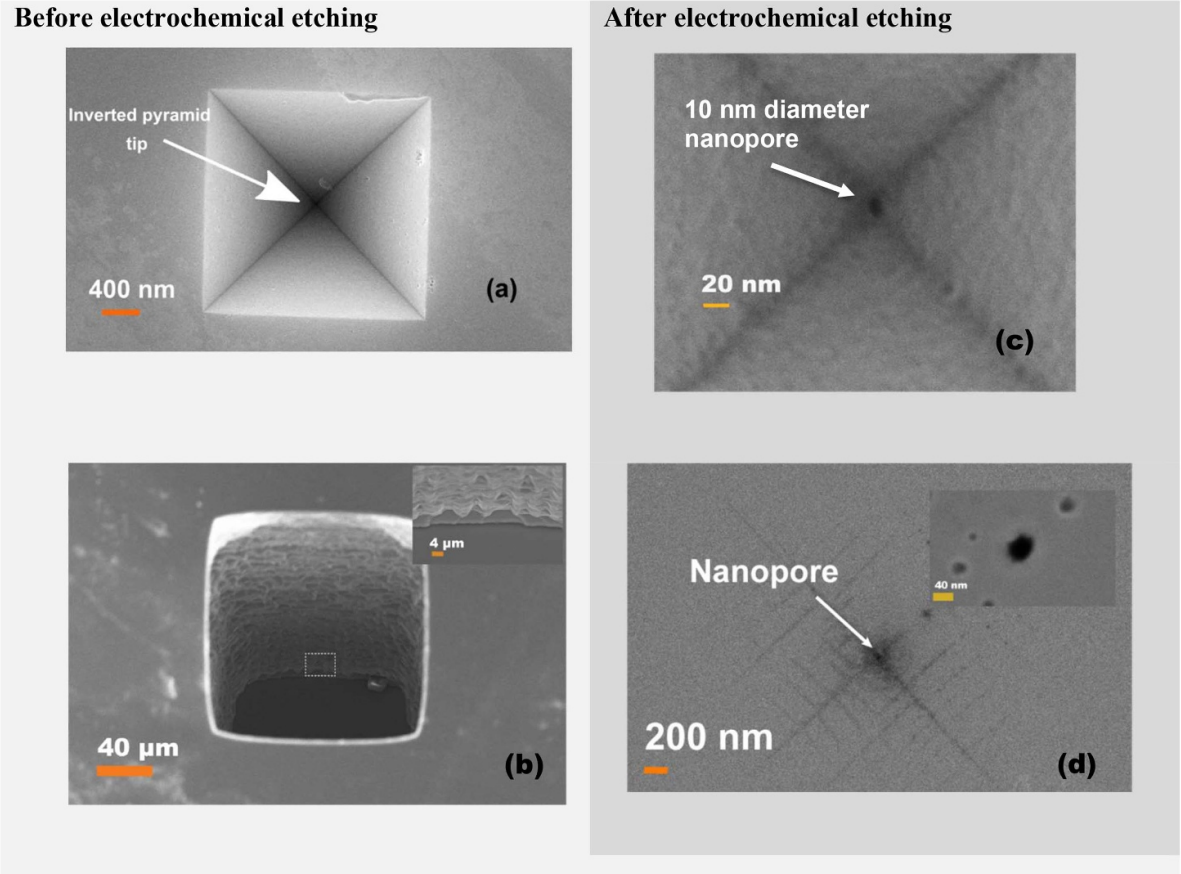

Figure 4. SEM images of the nanopore chip before and after electrochemical etching. (a) The top view of the rectangular opening with an inverted pyramid of the fabricated device layer after KOH etching. . An inverted pyramid cavity is formed due to the etch stop at <111> planes of the silicon. (b) Image from the handle layer showing the DRIE etched via hole. A closeup view of the image in the inset shows the SiO_2 layer and the scallops due to DRIE along the walls of the substrate indicating a complete etching of the substrate layer with a two-step process. (c) Processed nanopore at the bottom of the inverted pyramid with 10 nm diameter after electrochemical etching. (d) Image of the device layer as seen from the bottom side (handle layer). A nanopore from the substrate side indicates a successful electrochemical etching. The inset image shows a closeup view of the nanopore within the range of 30–40 nm in diameter.

decreased to a value of 10 V. During the transition phase from high voltage to low voltage, the current first peaks to a value of 30 μA and then decreases to a value of approx. 20 μA. A steady-state duration of a low bias region lasts for 7 min and ensures the formation of a high aspect ratio and smooth nanopore. However, careful control of the duration of the voltage bias is required to ensure a narrow pore. Appropriate control parameters among which the high bias voltage duration, slope and the low bias region are important, and influences on the diameter of these nanopores. By this method, nanopores of sizes of approximately 20 to 30 nm in diameter were obtained using optimized parameters. This method of processing nanopore is fast (8 min), and requires fewer control parameters than the previously described etching method which uses illumination to achieve breakdown [22].

The SEM images in figure 4 show the nanopore chip before and after electrochemical etching. Figure 4(a) shows a top view from the device layer of the pyramidal cavity after the silicon processing and before electrochemical etching. The 111 planes of silicon intersect to form a sharp-pointed apex of the pyramid as shown in the inset image. From the handle layer side, the SEM images in 4b and the close-up view shows a deep reactive ion etched (DRIE) square-formed hole with the exposed SiO_2 layer and the formation of the scallops along the walls indicate a complete etching of the handle layer revealing the suspended membrane. After electrochemical etching, the surface of the silicon becomes rough and a nanopore is formed at the bottom of the inverted pyramid as shown by the SEM image in figure 4(c). From the substrate side looking down to the device layer, the nanopore is visible indicating that the nanopore has been etched completely through the device layer and has a diameter in the range of 30–40 nm as visible in figure 4(d) and the inset image. The processing of many devices has consistently yielded single or arrays of nanopores in this diameter range as defined by the initial lithography step.

2.3. Nanopore DNA measurement set-up

A chip containing a nanopore with 10 nm to 30 nm diameter (figure 4) is placed in between the two chambers of a Teflon cell. The schematic of the biomolecule detection set-up is shown in figure 5. The chip is held by an O-ring and is tightly sealed to the Teflon cell. The chamber is filled with

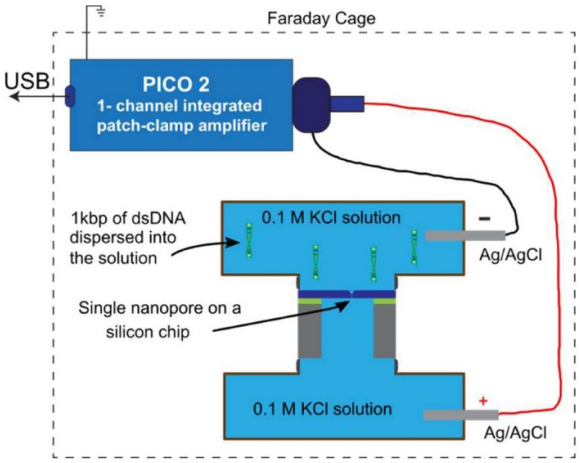

Figure 5. Experimental set-up for detection of individual DNA translocation events. A pico2 1-channel integrated patch-clamp amplifier is used for detection of ionic blockage current obtained from the DNA translocation. A solution of 0.1 M KCl is used as the electrolyte in the chamber. Two Ag/AgCl electrodes are inserted into each side of the chamber of the set-up. The set-up is enclosed in a faraday cage for noise isolation from external sources. The set-up is connected to a PC and the measurements are recoded using the instrument software.

0.1 M KCl solution on both sides. Before assembling, the chip is cleaned in oxygen plasma to improve the wettability of the chip surface. After assembling, trapped air bubbles are carefully removed from the membrane by insertion of buffer solution. Two Ag/AgCl electrodes (Alvatek LF1-45, UK) are connected to each of the chambers to create an electric field through a nanopore under applied bias and is also used for measuring the ionic current. A low-noise and low power voltage-clamp amplifier from Tecella (Pico-2, Tecella, US) is used to measure the ionic current through the pore. The data acquisition is set to 40 kHz sampling rate and recorded on a computer. To minimize external noise during measurement, the entire system of the amplifier and the Teflon cell is placed inside a Faraday cage.

2.4. Analysis of translocation events

The information about translocation events such as current blockade amplitude (I_b) dwell time ($t_{d,FWHM}$), and the relation between the dwell time and current blockade is analysed from the recorded data using custom Matlab® routines. The dwell time is the time related to the DNA translocating through the nanopore and it is defined as the full width half maximum (FWHM) of each translocating event. According to Pedone et.al, the FWHM value of the translocation of a DNA in a nanopore is the best represented time value since it avoids the erroneous calculation due to finite filter rise time and pulse dilation [30, 31]. In addition, only those events are counted which amplitudes are above the 3σ value from the baseline. This method of exclusion is required to avoid false detection of an event. Thus, short current spikes were avoided and not counted as a translocation event. The current blockade, I_b is defined as the difference between the ionic current at the local minima of an event and the average baseline value. The event charge deficit is given as, $ecd = \int_{event} I(t)\,dt$, where I(t) is the ionic current and dt is the time increment over the duration of an event and is given in kilo electron charge (ke) [32].

3. Results and discussion

The detection and analysis of dsDNA translocation through the silicon nanopore on SOI is presented and discussed. We demonstrate that a long and high aspect ratio nanopore typically gives longer translocation time that can be potentially used for single biomolecule detection purposes with lower bandwidth instruments.

3.1. Detection of dsDNA translocation in the nanopore

The measurement set-up for detection of translocation of individual dsDNA strands is described in the earlier section. The conductance of the nanopore is experimentally determined by varying the applied voltage (V_b) from 0 to ±800 mV in steps of 100 mV and calculated to be 0.02 μS at 1 M KCl. The measurement of a finite conductance also confirms the wetting of the nanopore. For the detection of dsDNA, a solution containing dsDNA with a concentration of 300 pM of 1000 bps length (Gene Technology Group, KTH, Sweden) is prepared and carefully dispersed in an 0.1 M KCl electrolyte on the negative potential side of the Teflon chamber as shown in figure 5. By varying the applied voltage bias after the dsDNA is dispersed into the solution, a threshold voltage of 300 mV is determined for the set-up. Below this voltage and at negative bias, no translocation of DNA occurs. Analysis of the DNA translocation through the nanopore is presented in figure 6. For DNA translocation trace recording, the voltage is increased to 800 mV and the ionic current is recorded for a duration of 300 s. After that current spikes are observed as shown in figure 6(a), ascribed to a current blockade obtained from the DNA translocation. The noise in the ionic current was estimated to be about 300 pA. The voltage was increased to 800 mV to have a better signal to noise ratio (approx. 2.5 times than at 300 mV) and allow more dsDNAs translocating per second.

The analysis results for translocation events occurring at 800 mV bias voltage is shown in figures 6(c) and (d). For example in one of the translocation events captured, it is assumed that the DNA enters the pore through one end of the DNA in and exits by the other end which could be inferred due to the constant current value of 1.6 nA for approx. 1.5 ms (figure 6(a) and inset) whereas in another event, it is speculated that the DNA may take up a coiled formation due to a shorter translocation time of approx. 500 μs [33]. The histogram analysis of dwell times gives us an average dwell time for the DNA in the solid-state nanopore of $t_{d,FWHM} = 1.1$ ms. Luo *et al* observed that the geometry of the nanopore, especially the length of the nanopore, plays an important role in slowing down the DNA [34]. With our silicon technology, the DNA translocation process is observed to be slower by 2–3 orders of magnitude compared to, e.g. thin silicon nitride membranes

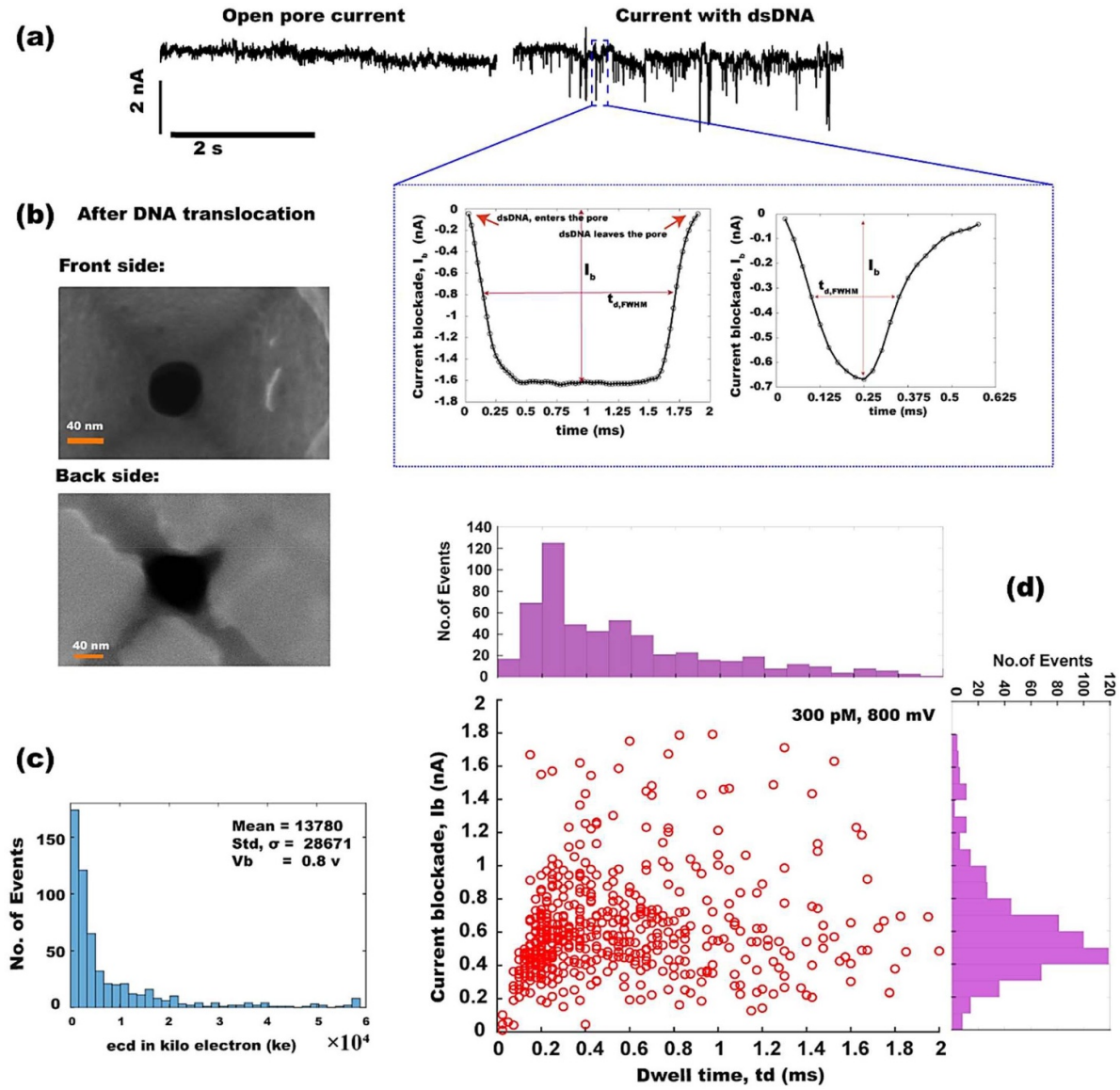

Figure 6. Analysis of DNA translocation events. (a) open pore current trace at 800 mV and after dsDNA is dispersed into the cis chamber. We observe a current spike for each DNA translocation event. The inset graph shows an example of two different types of DNA translocation events as detected by the silicon nanopore. One of the events has a wide dwell time upto 2 ms with a current blockade of approx. 1.6 nA and the other event has a shorter translocation time of . 0.6 ms with a current blockade of 0.7 nA. (b) SEM images of the front and back side of the nanopore after DNA translocation. The diameter of the nanopore is 60 to 70 nm. (c) Histogram plot of event charge deficit (ecd) in kilo electron charge. For 1kbps of dsDNA, a mean value of 13 780 ke can be calculated from the figure. (d) Scatter plot of all blockade events for blockade current versus dwell time. Shows the distribution from 0 to 2 ms dwell time of the DNA and 0 to 2 nA of the blockade current. Histogram plot of several events for different dwell times, t_{dFWHM}. From the graph, a mean value of the dwell time can be calculated to approx. 1.1 ms. Histogram of several events versus the corresponding current blockade, I_b. A mean value of the current blockade of about. 700 pA can be calculated from the figure.

[35]. However, with functionalized nanopores, it is reported that the DNA can be slowed down even more [36]. With our silicon technology, the DNA translocation process is observed to be slower by 2–3 orders of magnitude compared to, e.g. thin silicon nitride membranes [37]. However, with functionalized nanopores, it is reported that the DNA can be slowed down even more [38]. The SEM image of the nanopore After the DNA translocation events which was carried out for 300 s is shown in figure 6(b). From the figure, it is seen that the nanopore diameter is enlarged from 30–40 nm (figure 4(d)) to. 60–70 nm. Thus, the nanopore has enlarged by 20–40 nm at a rate of 4–8 nm min^{-1}. The slow etching of the silicon affected by the voltage bias caused a dynamic increase in nanopore diameter. One of the methods to mitigate the unwanted etching of the nanopore is to deposit a thin layer of dielectric around the nanopore. From the analysis, the average blockade current and the average event charge deficit is calculated to be approx. 700 pA and 13 780 kilo electron charge (ke) as shown in figures 6(c) and (d), respectively. The distribution of the dwell time and the blockade current is plotted as a scatter plot in figure 6(c). We speculate the broad span of dwell time and ionic current blockade might be due to the large variation

in the molecular shape during translocation. The span of the dwell time and the blockade current is from 0 to 2 ms and 0 to 2 nA. We can see that there is a positive correlation between the dwell time and the current blockade.

It was observed that for 1200 mV (not shown), the translocation rate was calculated to be 60 translocations s^{-1} and for 800 mV the translocation rate of approx. 15 translocations sec^{-1}. The increase in the number of events with bias confirms the single-molecule origin of the translocation. The capture volume increases with a higher bias resulting in a larger translocation rate for a given DNA concentration. The inverted pyramid could act as a micro funnel that guides the DNA into the access region of the nanopore. Therefore, our novel design of a combination of an inverted pyramid together with the long nanopore proves an efficient and effective way of DNA translocation detection.

4. Conclusion

In summary, we have demonstrated single nanopore fabrication on a wafer-scale. For our process, we produced twelve wafers in four batches with 26 devices per wafer in total. The devices had 15 mm × 15 mm in dimension and contained single nanopores as well as array of nanopores. The wafer level fabrication of SOI wafer yielded about 60%–70% with the diameter in the range of 10 nm to 50 nm. The characterized single nanopore chip had a high aspect ratio, with a range of 30–40 nm diameter and approx. 700 nm long nanopore processed on an SOI wafer followed by electrochemical breakdown etching. A repeatable and stable process flow is demonstrated. The solid-state nanopores thus obtained was successfully tested for 1kbps dsDNA translocation. The dwell time for one translocation of dsDNA is measured to be approx. 0–2 ms and is significantly slower than a typical silicon nitride nanopore. The demonstrated concept is advantageous for biomolecule sensing allowing for better control of the analyte-nanopore interaction. The plan is to further increase the length of the nanopore and to determine the translocation time for various lengths of DNA. Also, to functionalize the inner diameter of the nanopore for further slowing down the DNA molecule. Besides, we plan to utilize the functionalized surface to study the biomolecule behaviour of binding and unbinding from the surface through the conductance measurements.

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